DOCID: 3928944
Approved for release by NSA on 12-01-2011, Transparency Case# 63852

An Evaluation of Conventional and LDD Devices for Submicron Geometries (U)

STATUTORILY EXEMPT

As transistor dimensions shrink, lightly-doped drain (LDD) device structures are expected to improve MOSFET reliability at the expense of current drive due to parasitic source/drain resistance. In this study, both conventional and two types of LDD processes are evaluated in terms of parametric data and hot carrier degradation. Optimized LDD devices can be expected to achieve one to three orders of magnitude lifetime increase when compared to conventional n-channel MOS transistors with equal current drive.

INTRODUCTION

As transistor dimensions shrink to below one micron, various high field effects in silicon devices create reliability problems. Among these are electromigration, time-dependent dielectric breakdown, and hot carrier injection. Processing and design changes are made to reduce the possibility of circuit failure resulting from these mechanisms. The introduction of lightly-doped drain (LDD) structures is expected to decrease MOS device susceptibility to hot carrier effects. Device simulations have shown that the LDD process reduces peak electric fields in the transistor and also shifts the location of these peak fields [1,2]. It is expected that these changes will result in less hot carrier injection into the channel oxide, thus increasing device lifetimes. However, some evidence indicates LDD devices exhibit increased degradation under DC stress conditions due to drain modulation by injected carriers [3,4]. The increased parasitic resistance of the lightly-doped regions also reduces current drive capability when compared to conventional MOS transistors. Therefore, the use of LDD structures must be evaluated carefully to ensure that it meets both parametric and reliability requirements. In this paper, a comparison of conventional and two types of LDD devices is made.

EXPERIMENTAL DETAILS

Figure 1 shows the process steps necessary to fabricate the LDD structure. After polysilicon gate definition, a low dose implant forms the N^- region. A CVD oxide is deposited which smooths the topography such that the oxide is thicker over the edges of the gate. This oxide is then etched, leaving a *spacer* oxide on the sides of the polysilicon. A heavier dose implant then forms the N^+ source/drain regions. It should be noted that the LDD process needs no extra mask levels and is compatible with a self-aligned silicide (SALICIDE) fabrication sequence. The critical parameters in the LDD formation are the spacer width and N^- implant conditions, as these will determine the location and magnitude of the peak electric fields in the device. Optimization of these quantities will result in acceptable device characteristics while increasing reliability. For this study, two spacer lengths with different implant energies were used. Table I gives some process values for the three types of devices (CONV, LDD1, LDD2) fabricated. Measurements of

~~FOR OFFICIAL USE ONLY~~

Table I
Processing information for the three device types used in this study.

	CONV	LDD1	LDD2
T_{ox} (nm)	19	19	19
Spacer (μm)	None	0.1	0.15
N^- dose (#/cm²)	None	1×10^{13}	1×10^{13}
N^- energy (keV)	None	30	45

parasitic resistance and effective channel length indicate that the N^- length for the LDD1 transistor is very small (<0.10 μm total) due to spacer thinning and lateral diffusion of the N^+ implant during subsequent processing. The combined N^- length for the LDD2 device is expected to be ~0.15 μm.

PARAMETRIC RESULTS

Figure 2 shows the n-channel punch-through voltage V_{pt} (defined as V_{ds} for $I_{ds}=1\mu A/\mu m$ of width) for the CONV, LDD1, and LDD2 transistors. The LDD devices have slightly larger V_{pt} at larger mask lengths than conventional devices and do not show as dramatic a roll-off for $L_{mask}<1.0$ μm. Figure 3 shows substantially the same behavior for the n-channel threshold voltages. Figure 4 shows the saturation current I_{dss} ($V_{gs}=V_{ds}=5$ volts), indicating that the LDD structures reduce current drive by 15–25 percent for $L_{mask}<1.0$ micron. Coincidentally, the 0.6 μm LDD devices have I_{dss} approximately equal to the 0.8 μm conventional MOSFET. Linear transconductance values are 7–15 percent lower for LDD1 and LDD2, as shown in figure 5. Figure 6 shows that n-channel subthreshold slope values are similar for all types of devices. However, the substrate current is much higher for the conventional transistors, as seen in figure 7. At $L_{mask}=0.6$ μm, the LDD1 and LDD2 structures reduce substrate current (I_b) by 83 percent and 90 percent, respectively. Figure 8 plots I_b/I_{dss}, a number which is sometimes used to indicate peak electric fields [4]. This value is reduced by a factor of four and ten for the two LDD types at $L_{mask}=0.6$ μm.

HOT CARRIER STRESS CONDITIONS

DC hot carrier stresses for $t=10^5$ seconds and $V_{ds}=4,5,6,7,8$ volts with V_{gs} adjusted for maximum I_b were applied to the three types of n-channel devices with L_{mask} ranging from 0.5 to 1.0 microns. Not all combinations of stresses were done, but each type of structure (CONV, LDD1, LDD2) was stressed to achieve a wide range of I_b. In all, 60 devices representing 12 variations were stressed. The degradation of five device parameters was

fitted to a power-law relationship [5] so that device lifetimes (τ_{dc}) could be calculated. The five parameters monitored were

- I_{dsf} : Forward mode I_{dss} ($V_{gs} = V_{ds} = 5$ volts)
- I_{dsr} : Reverse mode I_{dss}
- G_m : Linear transconductance (maximum slope of $I_{ds} - V_{gs}$) at $V_{ds} = 50$mV
- V_t : Linear threshold voltage found by maximum slope technique at $V_{ds} = 50$mV
- S_{vt} : Subthreshold slope (inverse of maximum slope of Log $I_{ds} - V_{gs}$) at $V_{ds} = 50$mV

Forward and reverse modes indicate current flow directions with respect to I_{ds} during stressing. Degradation of G_m, V_t, and S_{vt} was equal in both forward and reverse directions under all stress conditions used. Device lifetime was defined as the time at which 10 percent or 10mV change in the parameter occurred. This lifetime has been modeled as [5]

$$\tau_{dc} = A * I_b^{-m}$$

(equation 1)

or taking the log of both sides,

$$\log(\tau_{dc}) = \log(A) - m \log(I_b)$$

(equation 2)

Recent work indicates that this model holds for similar device types regardless of the effective channel length or applied biases during stress for L_{eff} = 0.6-2.0 µm and V_{ds} in the range 4–7 volts [6,7].

Table II

Results of linear regression fitting of degradation data to eq [2], $\log \tau_{dc} = \log A - m \log I_b$.

	CONV		LDD1		LDD2	
	m	Log A	m	Log A	m	Log A
I_{dsf}	2.6	12.9	2.6	12.9	2.6	12.9
I_{dsr}	2.5	10.6	2.6	10.4	2.4	10.8
V_t	1.9	7.7	2.0	7.7	2.3	9.9
G_m	2.8	9.5	2.9	10.3	2.6	9.9
S_{vt}	2.8	10.9	2.6	10.2	3.0	13.3

RESULTS AND ANALYSIS

Log (τ_{dc}) vs log (I_b) plots were made for each of the five parameters (see figs. 9–13). The data points shown are averages for 3–5 devices. Calculation of m and log (A) values was done by linear regression analysis applied to equation 2. Results of the regression fitting for each device type and parameter are given in Table II. The slope values (m) are in the range of 1.9–3.0, centering around 2.6, which is in general agreement with published data for both conventional and LDD devices [6,7]. The values for the LDD1 device degradation fit are very close to those found for the conventional MOSFETs for all five parameters measured. The LDD2 structures have similar rates of degradation for I_{dsf} and I_{dsr} but quite different for V_t and S_{vt}. The G_m values may be slightly different for the LDD2 transistors. The LDD1 similarity to CONV in terms of hot carrier degradation is attributable to the fact that the LDD1 devices have short N^- regions. Therefore, charge injection due to hot carriers in the LDD1 structure will be in or very near the oxide under the gate, similar to conventional devices, creating parameter changes comparable to conventional devices. To understand the LDD2 behavior, an examination of the hot carrier injection process is beneficial.

Hot carrier degradation has been attributed to both holes and electrons being injected into the oxide. The theory proposed is that the electrons are trapped at existing sites in the oxide, probably very near or at the interface, and also at new traps created by the injected holes [8,9]. These trapped electrons will shift V_t to a more positive value and also reduce I_{dss}. The asymmetry of the distribution of the additional trapped charge explains the differing degradation of I_{dsf} and I_{dsr} [4,10]. The subthreshold slope is increased due to increased interface traps [11]. Mobilty values (and therefore G_m) are lowered because both the traps and trapped charge create more scattering sites along the channel for the current carriers [9,11].

The different degradation of CONV and LDD2 transistors is due to the different location in the oxide of these traps and charges with respect to the drain junction. For conventional devices, the carrier injection occurs under the gate near the drain and can subsequently affect channel surface potential, while in typical LDD transistors the injection largely occurs outside the gate edge in the oxide above the N^- region (1). Therefore, parameters which monitor changes in channel surface potential as a function of gate bias will be less affected in the LDD2 devices even with the same amount of hot carrier injection (I_b). V_t and S_{vt} are parameters which measure this. I_{dsf} degrades similarly for both device types because the charges are generally confined to the *pinch-off* region in a conventional MOSFET, so that for either structure it is the drain depletion region field which accounts for the charge. The reverse I_{dss} is reduced equally for both because the effect of the charge is the same: reduction of mobile carrier concentration at a given (V_{gs},V_{ds}) bias condition. Conventional devices have reduced channel carrier concentration, while LDD2 devices have reduced N^- region carrier concentration. This is the so-called hot carrier drain modulation [3]. Even though in the LDD2 structure the extra trapped charges and interface traps are in the oxide above the N^-, they still create additional scattering sites for the current carriers, so that G_m reduction is similar. For the LDD2 device, the G_m degradation may be slightly smaller which can be attributed to current spreading as it enters the N^- region. Fewer carriers to scatter at the surface will mean less G_m reduction for the same I_b.

The data indicates that device lifetimes do follow [2], so that log τ_{dc} values at $V_{dd}=5$ volt operation can be calculated from accelerated stress testing. Table III gives predicted lifetimes for each of the five parameters and three device types for $L_{mask}=0.6$ and 0.8 microns at $V_{dd}=5$ volts.. Recall that I_{dss} values for 0.6 µm LDD and 0.8 µm CONV devices

Table III
Predicted log lifetimes (in seconds) for L_{mask} = 0.6 and 0.8 µm, assuming V_{dd} = 5 volts.

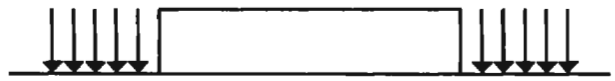
	CONV		LDD1		LDD2	
L_{mask}	0.6 µm	0.8 µm	0.6 µm	0.8 µm	0.6 µm	0.8 µm
I_{dsf}	6.6	8.0	8.6	9.0	9.2	9.8
I_{dsr}	4.5	5.9	6.1	6.5	7.4	8.0
V_t	3.1	4.1	4.4	4.7	6.6	7.2
G_m	2.7	4.2	5.5	6.0	6.2	6.8
S_{vt}	4.1	5.6	5.9	6.3	9.1	9.8

were nearly identical, so that comparing these transistors indicates reliability improvements using an LDD without sacrificing current drive. The 0.6 µm LDD2 device τ_{dc} is 1.2–3.5 orders of magnitude greater for the various parameters when compared to the 0.8 µm CONV transistor.

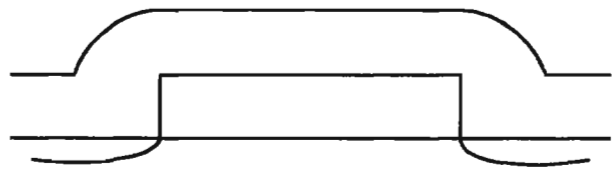
SUMMARY

As MOSFET dimensions shrink, LDD device structures are expected to improve device reliability. In this study both conventional and two LDD structures are evaluated in terms of parametric data and hot carrier degradation. It is shown that LDD processing improves parameter control as the channel length decreases, but it reduces saturation current by 15–25 percent. Indicators of hot carrier creation (I_b, I_b/I_{dss}) show a substantial reduction for LDD transistors. DC hot carrier stress results indicate that parameter lifetimes for all transistor structures do follow the simple models proposed by other authors, but that some parameters (V_t, S_{vt}) degrade differently even under equal I_b stressing. This is explained by noting the change in the location of hot carrier injection for conventional versus LDD transistors. Optimized LDD devices can be expected to show improved lifetimes even when compared to conventional MOSFETs with equivalent current drive.

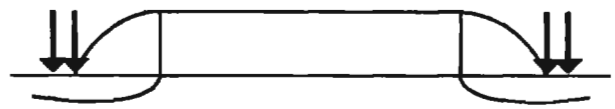
~~FOR OFFICIAL USE ONLY~~



a) N^- implant



b) CVD oxide deposition



c) N^+ implant

d) Finished LDD device

Fig. 1. Process steps required to form n-channel LDD device.

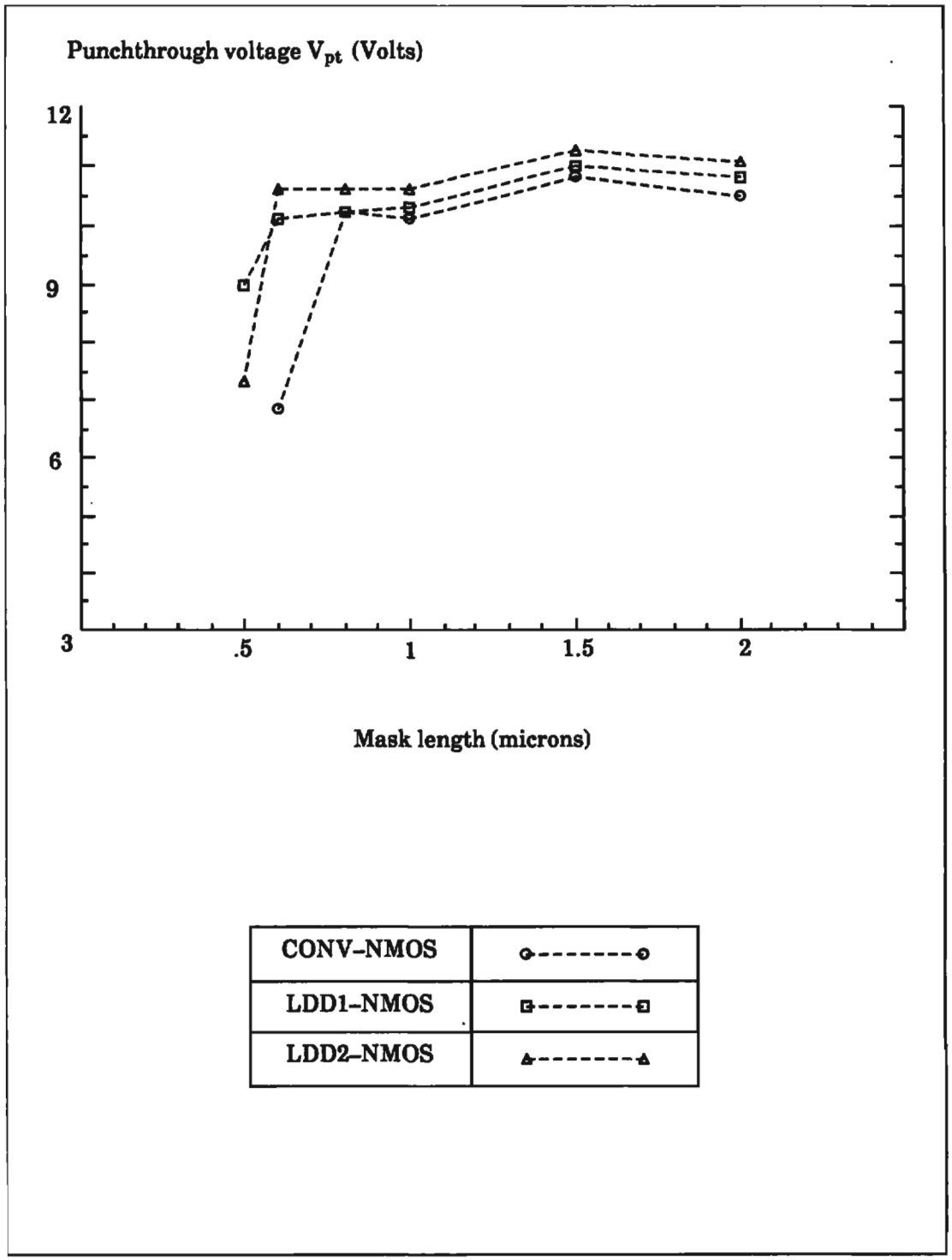


Fig. 2. Voltage (I_{ds} = 1μA/μm width) vs L_{mask} for n-channel devices.

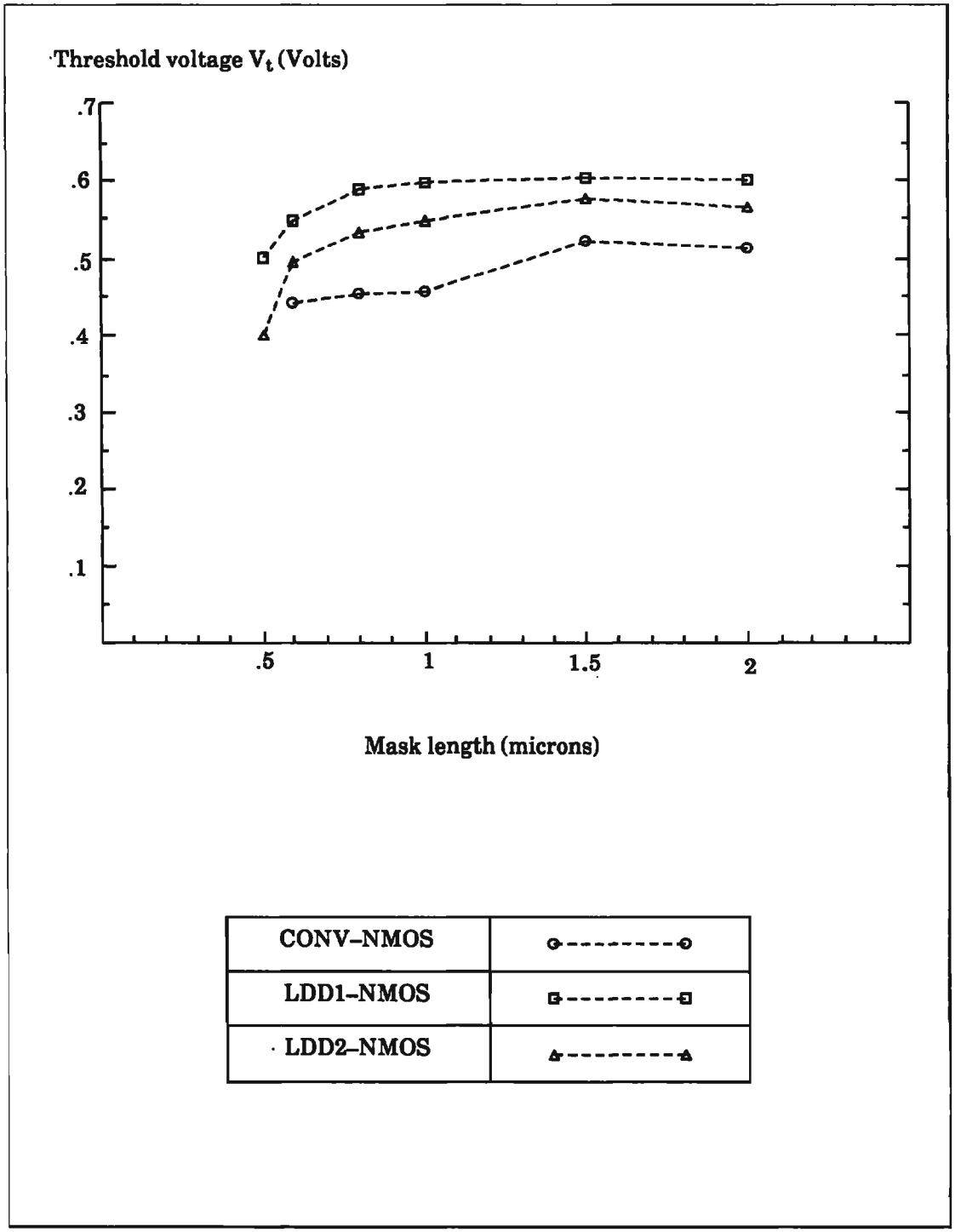


Fig. 3. Threshold voltage vs L_{mask} for n-channel devices.

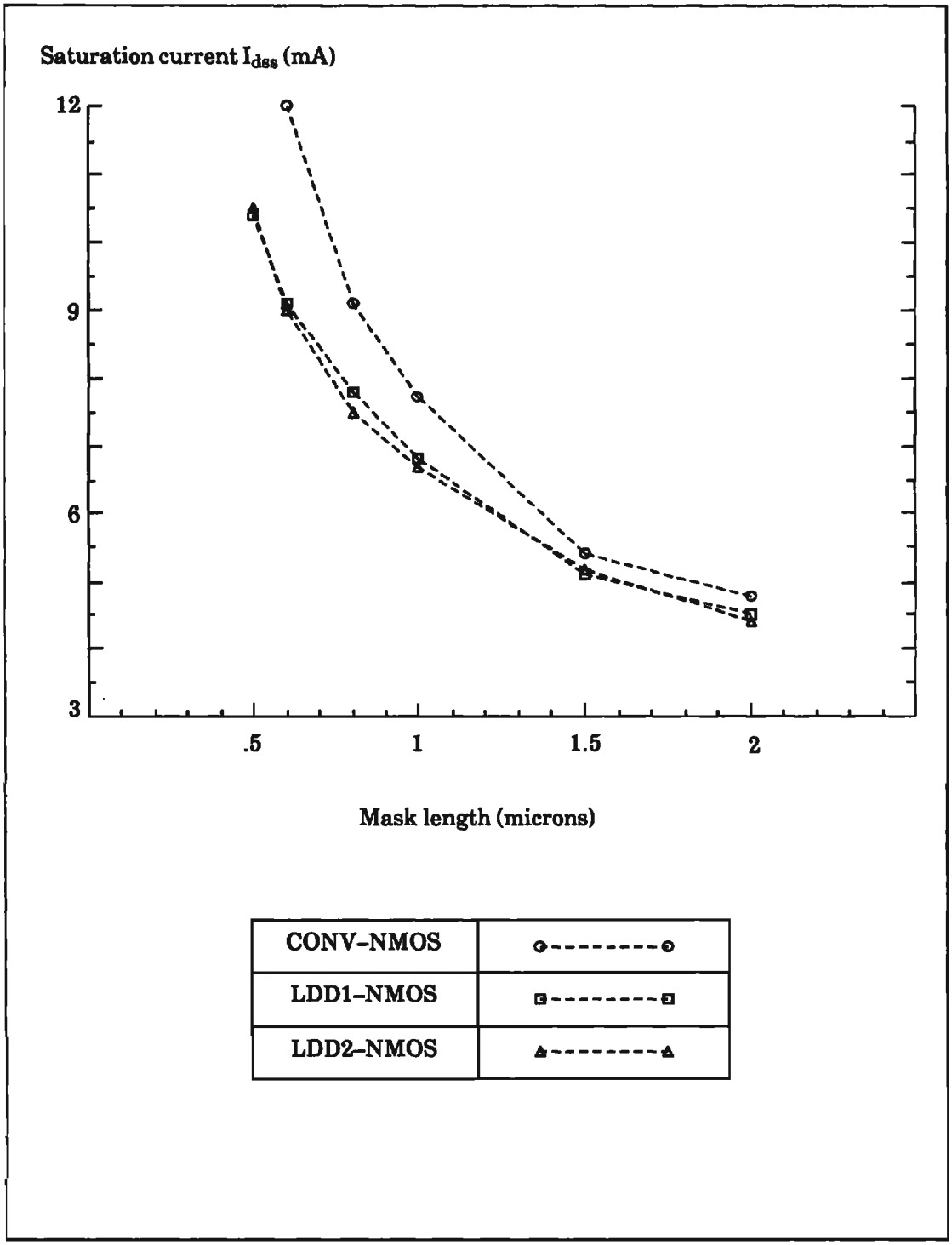


Fig. 4. Saturation current (V_{gs} = V_{ds} = 5 volts) vs L_{mask} for n-channel devices.

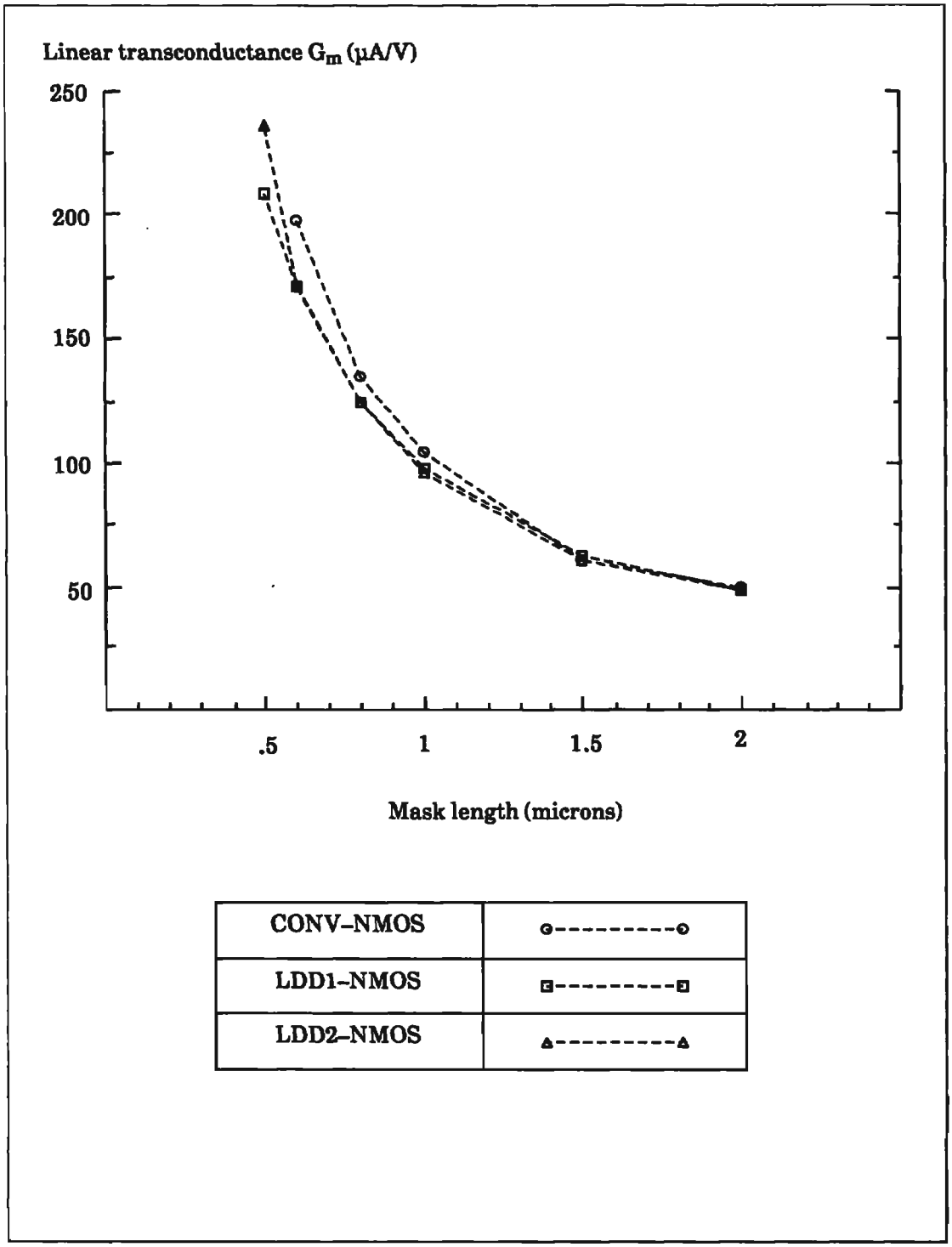


Fig. 5. Transconductance ($G_m = \Delta I_{ds}/\Delta V_{gs}$) vs L_{mask} for n-channel devices.

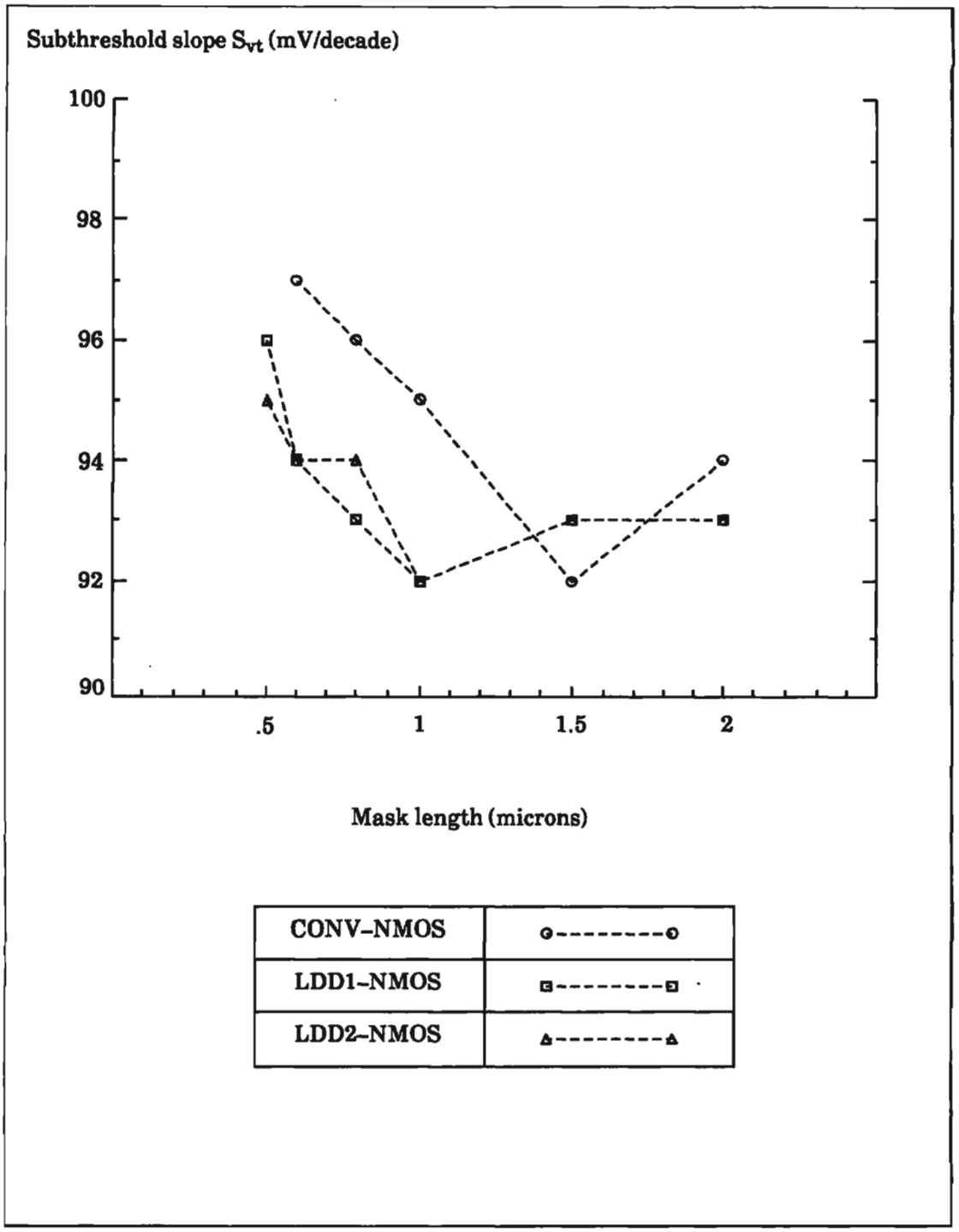


Fig. 6. Subthreshold slope vs L_{mask} for n-channel devices.

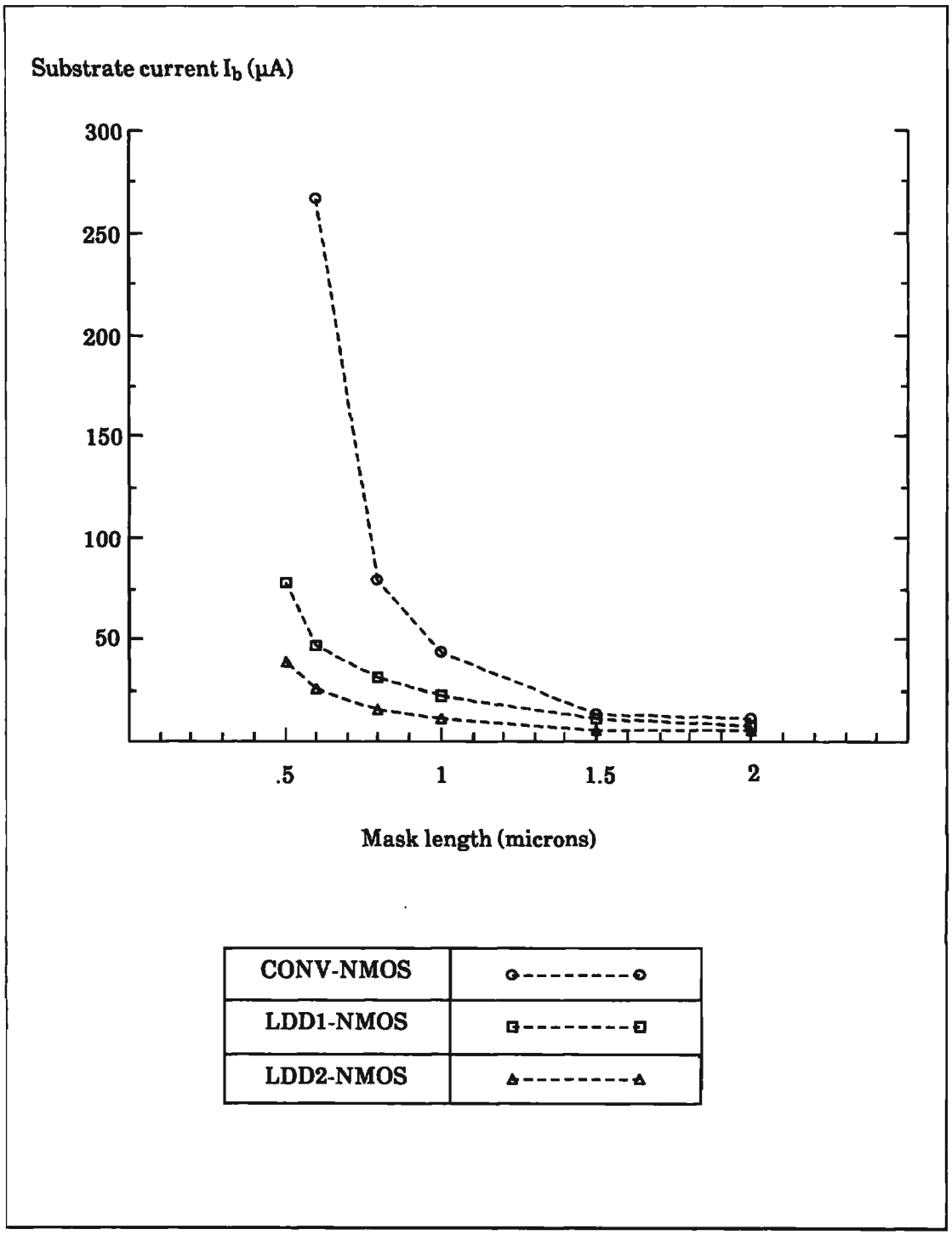


Fig. 7. Maximum substrate current (V_{ds} = 5 volts) vs L_{mask} for n-channel devices.

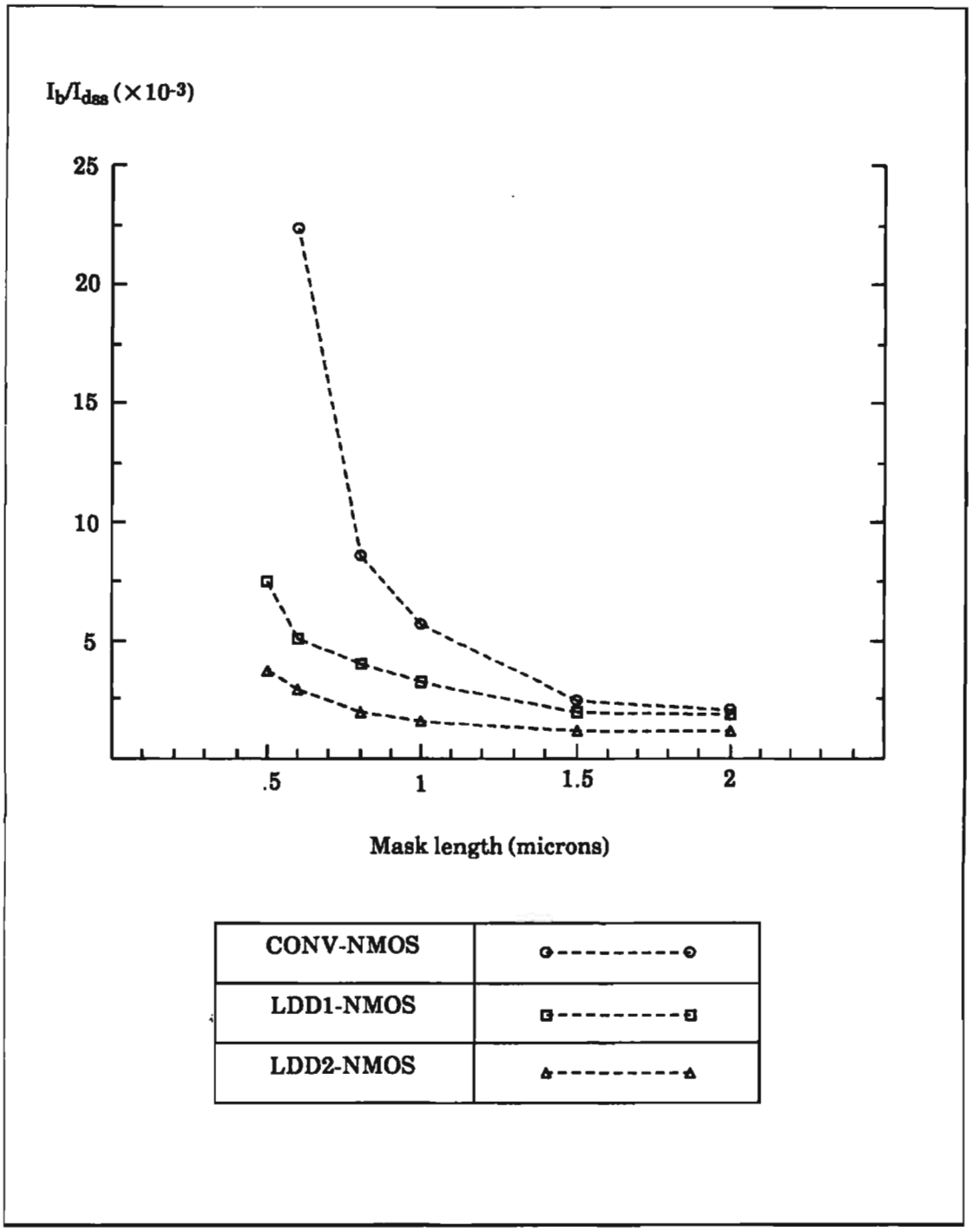


Fig. 8. Peak electric field indicator I_b/I_{dss} vs L_{mask} for n-channel devices.

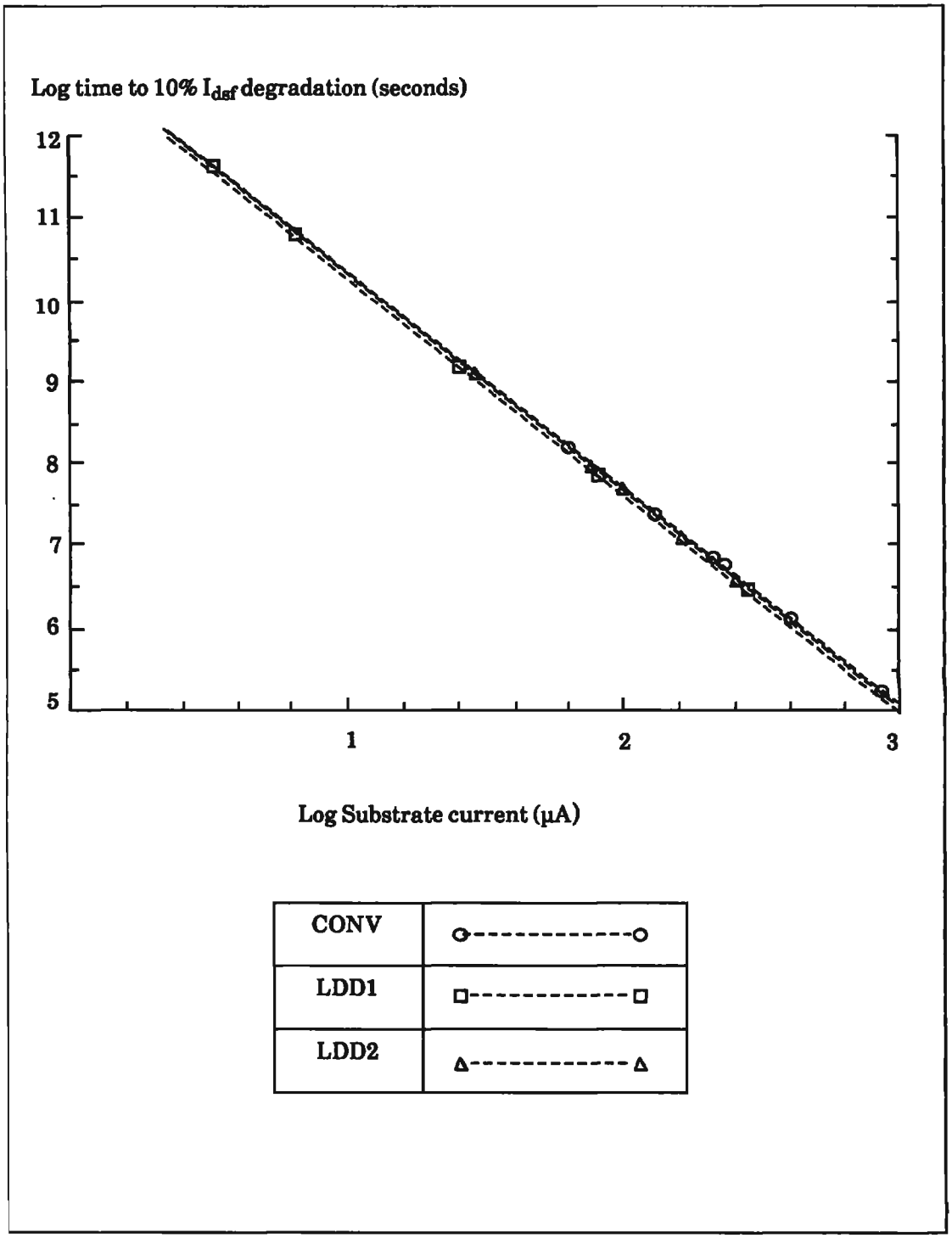


Fig. 9. Log I_{dsf} lifetime vs Log I_b with regression fit lines.

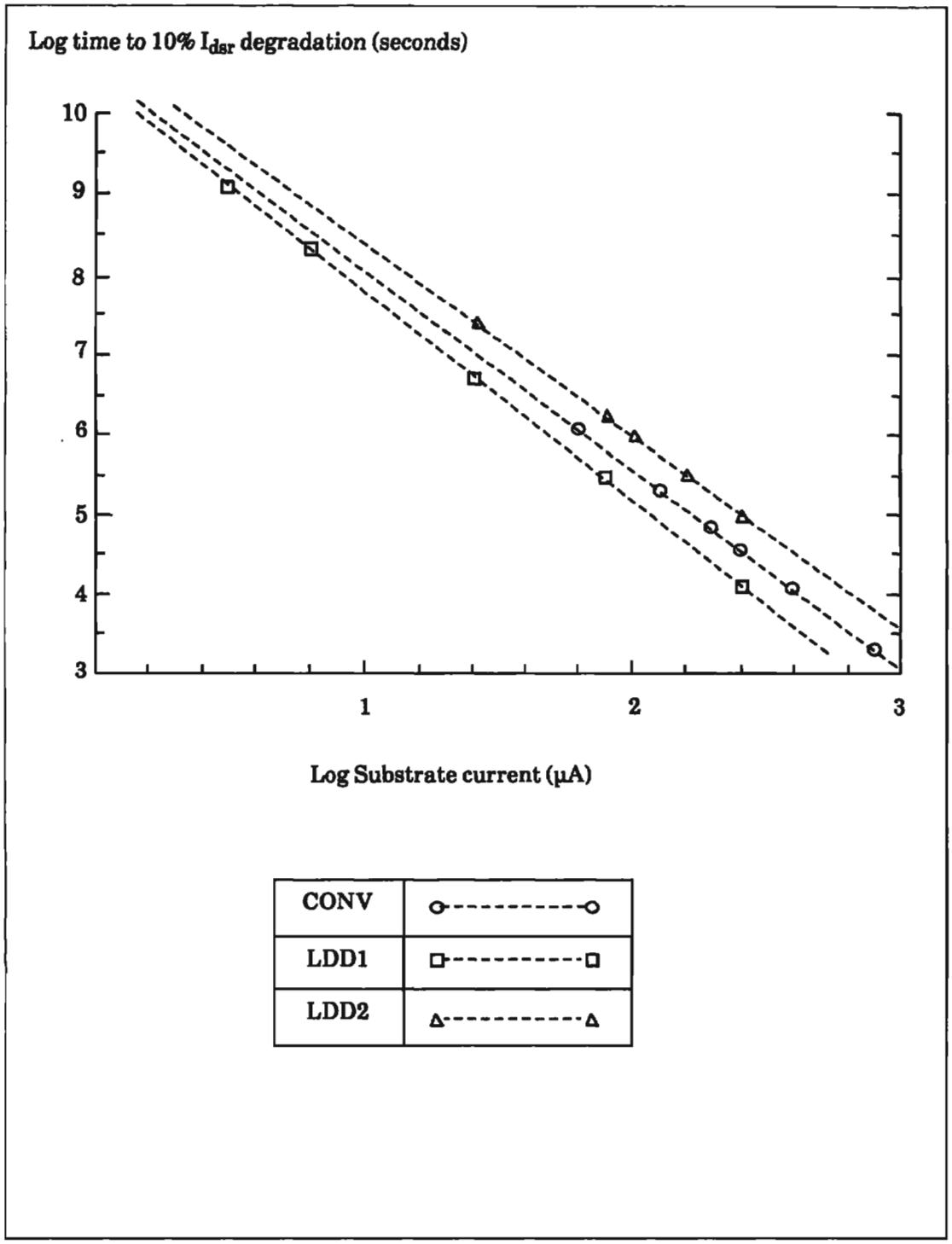


Fig. 10. Log I_{dsr} lifetime vs Log I_b with regression fit lines.

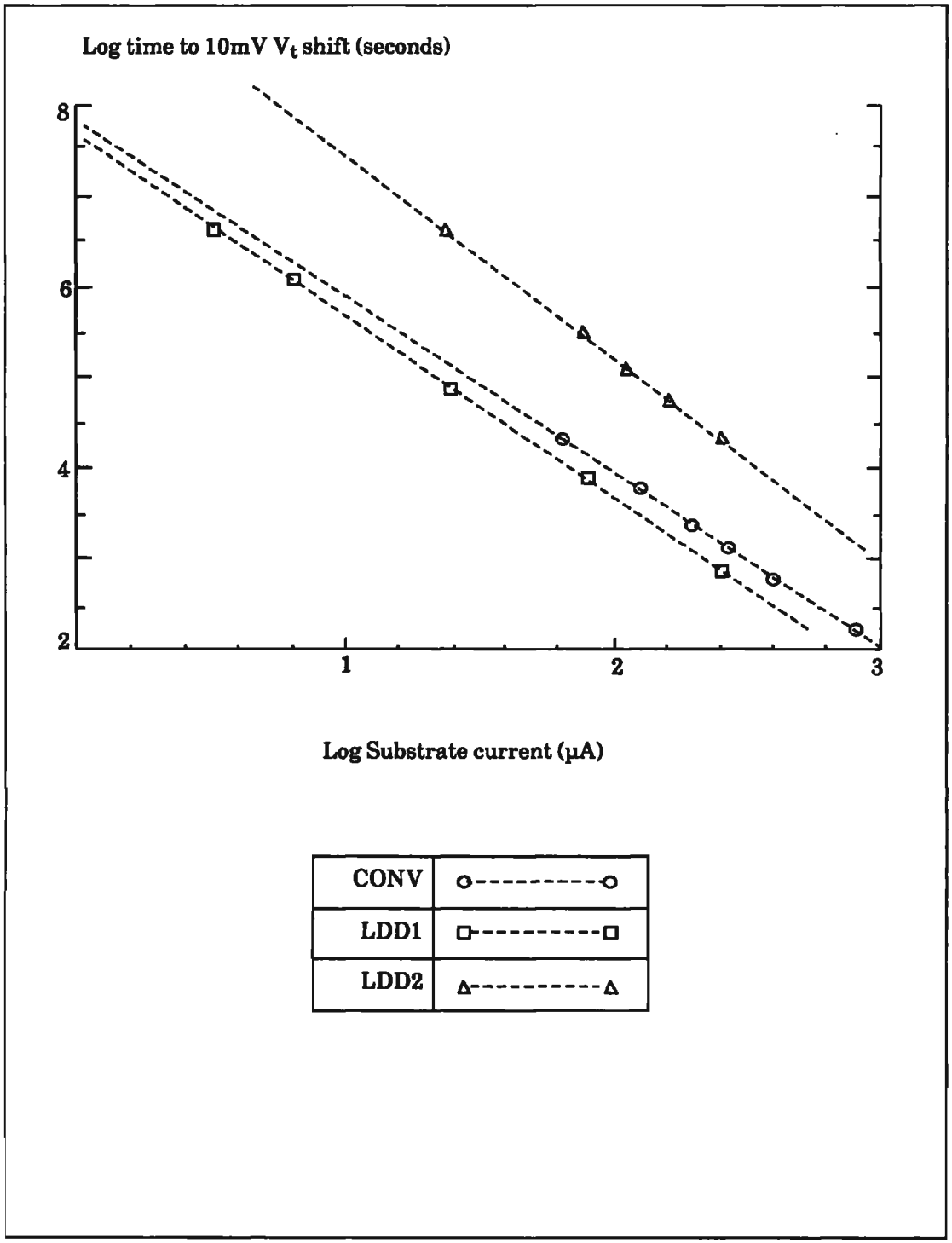


Fig. 11. Log V_t lifetime vs Log I_b with regression fit lines.

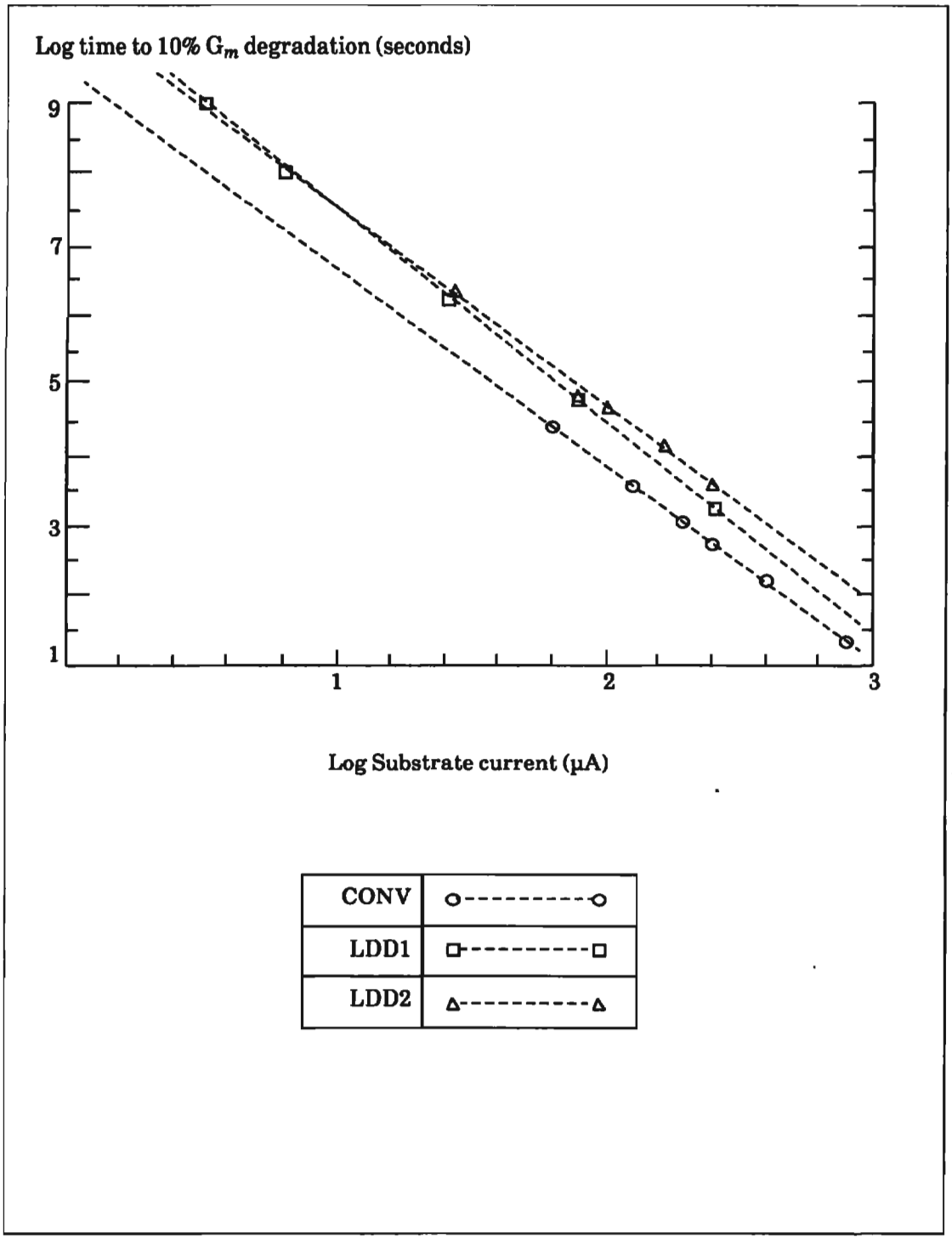


Fig. 12. Log G_m lifetime vs Log I_b with regression fit lines.

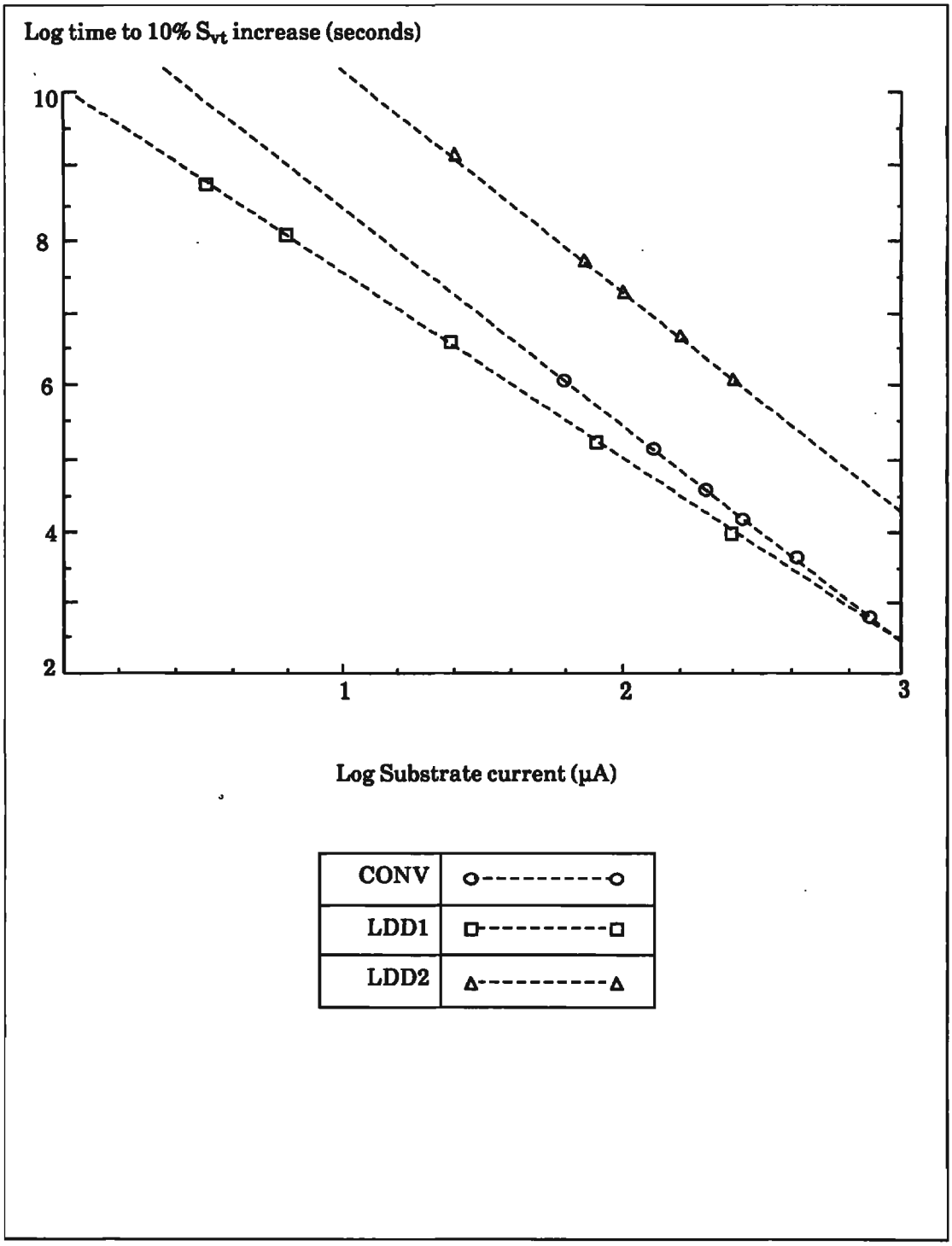


Fig. 13. Log S_{vt} lifetime vs Log I_b with regression fit lines.

STATUTORILY EXEMPT

REFERENCES

[1] Sangiorgi, E., et al. "A Hot Carrier Analysis of Submicrometer MOSFET's," *IEEE Electron Device Letters*, Vol. 9, 1988, p. 13.

[2] Toyoshima, Y., et al. "Mechanism of Hot Electron Induced Degradation in LDD NMOSFET," *IEDM Technical Digest*, 1984, p. 786.

[3] Hsu, F.C., and H.R. Grinolds. "Structure Enhanced MOSFET Degradation Due to Hot-Electron Injection," *IEEE Electron Device Letters*, Vol. EDL-5, 1984, p. 71.

[4] Wei, C., J. Pimbley, and Y. Nissan-Cohen. "Buried and Graded/Buried LDD Structures for Improved Hot-Electron Reliability," *IEEE Electron Device Letters*, Vol. EDL-7, 1986, p. 380.

[5] Takeda, E., and N. Suzuki. "An Empirical Model for Device Degradation Due to Hot Carrier Injection," *IEEE Electron Device Letters*, Vol. EDL-4, 1983, p. 111.

[6] Horiuchi, T., et al. "A Simple Method to Evaluate Device Lifetime Due to Hot-Carrier Effect Under Dynamic Stress, "*IEEE Electron Device Letters*, Vol. EDL-7, 1986, p.337.

[7] Mikoshiba, H., T. Horiuchi, and K. Hamano. "Comparison of Drain Structures in N-Channel MOSFET's," *IEEE Transactions on Electron Devices*, Vol. ED-33, 1986, p. 140.

[8] Bellens, R., et al. "Hot-Carrier Effect in N-Channel MOS Transistor Under Alternating Stress Conditions," *IEEE Electron Device Letters*, Vol. 9, 1988, p. 232.

[9] Takeda, E., A. Shimizu, and T. Hagiwara. "Role of Hot-Hole Injection on Hot-Carrier Effects and the Small Degraded Channel Region in MOSFET's," *IEEE Electron Device Letters*, Vol. EDL-4, 1983, p. 329.

[10] Hui, J., and J. Moll. "Submicrometer Device Design for Hot-Electron Reliability and Performance," *IEEE Electron Device Letters*, Vol. EDL-6, 1985, p. 350.

[11] Baglee, D., et al. "Lightly Doped Drain Transistors for Advanced VLSI Circuits," *IEEE Transactions on Electron Devices*, Vol. ED-32, 1985, p. 896.