REF ID:A71743

MEMO ROUTING SLIP

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	INITIALS		
1 NAME OR TITLE MR. RAY L. BOWMAN			CIRCULATE
ORGANIZATION AND LOCATION R/D 353	DATE		COORDINATION
2			FILE
			INFORMATION
3			NECESSARY ACTION
			NOTE AND RETURN
4			SEE ME
			SIGNATURE

REMARKS

I looked over your Volume 1 on DERVISH and am impressed with the excellence of the work done thus far to explain the theory and general operative nature of the gadgetry. I shall look forward to receipt of successive volumes. Congratulations on Vol. 1 to all concerned in its production.

FROM NAME OR TITLE J. W. Friedman

DATE 21 June 1944

ORGANIZATION AND LOCATION

DD FORM 1 FEB 50 95 Replaces DA AGO Form 895, 1 Apr 48, and AFHQ Form 12, 10 Nov 47, which may be used. 16—49487-4 GPO

STANDARD FORM NO 64

Office Memorandum • UNITED STATES GOVERNMENT

TO Mr Friedman, Special assistant DATE 10 June 1954

FROM Mr Bowman, R/D 353

SUBJECT DERVISH

In view of your professional and personal interest in certain phases of our work in R/D 35 it seems fitting to send you a copy of the DERVISH description now being distributed. I hope this will serve in a small way to give you information concerning our present endeavor

Ray L Bowman

TOP SECRET

DERVISH

General Description

Volume 1 1 June 1954

Copy No. 6

Task No. 353-7406

By: Ray L. Bowman
Ray L. Bowman
R/D-353

Control No. 346/6

30 775

TOP SECRET

PREFACE

The purpose of this document is to disseminate to interested and key personnel the general philosophy of DERVISH and descriptions of units developed thus far The aim is two-fold (1) To acquaint machine-minded analysts with some of the applications and programming aspects of the DERVISH units, and (2) To acquaint technical personnel briefly with the theory and logic of operation

The units discussed in this volume represent a result of ideas advanced in NSA-35 and NSA-06 They follow one line of development mostly, although other lines are being considered on a lower priority because of the emphasis being placed upon getting a few assemblies of units into operation Local effort is being augmented by a time and materials contract

The author gratefully acknowledges the efforts of and contributions to this task by C J Schierlmann, R E Gordon, W McGough, Jr , and L W Lathroum of NSA-35, D A Shepard and E D Marston of NSA-06

R L B

TABLE OF CONTENTS

CHAPTER I

GENERAL DESCRIPTION

I Introduction

DERVISH, a sub-project approved 4 December 1951 by DIRAFSA, is directed toward a building block philosophy of analytic machine assembly and re-assembly with particular emphasis on rotor solution devices These building blocks are not necessarily assumed to be repetitive circuits or modules designed to facilitate production line construction and standardize plug-in units, but are to be considered more as functional blocks which may be assembled in most any arrangement to perform a set or sequence of logical operations and yet possess many desirable maintenance features Each block is to have facility for performing a specific unique function This idea is not new, neither has it been fully exploited Engineering effort devoted to the development of a family of building blocks has indicated a favorable degree of practicability of this philosophy The growth of DERVISH stems from the construction and demonstration during July - November 1951 of a unit applying dynamic circuit techniques to an arithmetic representation of a wired rotor which handled characters at a rate of 167,000 per second. From this, it was evident that other functional blocks could be built to perform functions of addition, subtraction, storage, substitution, selection, etc , at the same rate of speed

This building block philosophy has a number of distinct advantages over present approaches to machine design and construction in that a new special purpose device can be assembled in a matter of weeks by no more than a half dozen laboratory technicians As soon as the device has served its purpose, it can be readily changed, modified or dismantled and the units made available for the assembly of another device In this manner the normal two to three years' delay encountered between a request for a machine and its realization would be effectively eliminated

II. Objectives

One of the major objectives in the development of these units is to make them of such nature that an analyst with a general knowledge of machine aid techniques can make a functional layout of a machine in block diagram form. By use of the building blocks, the engineering effort required for the realization of the device can be narrowed down to a smaller scope than would be possible normally and the time required to construct a piece of equipment and get it into operation is substantially reduced

Another objective is to make the units mutually compatible circuit-wise and yet be flexible and adaptable to a variety of applications. To achieve this, a pulse timing standard has been established for the input and output of units and extra control leads are provided where possible so their versatility may be increased.

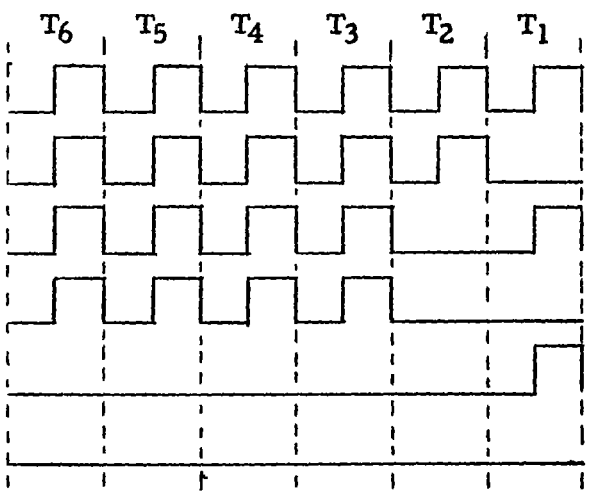
In order that equipment down time be minimized and maintenance and repair simplified, the chassis are of a plug-in design which permits rapid replacement of faulty ones The component layout has been made in such a manner that all elements are readily accessible for trouble shooting and replacement

III Notation and Representation

In the DERVISH units characters, numbers and quantities are represented in a serial binary form. Some units utilize 5-bit quantities and others 6-bit quantities but all are based on a 6-bit cycle In the normal concept a binary quantity of 1's and 0's is represented by pulses and no pulses respectively, but a one's complement or dual representation is employed in these units In effect, this means that normal logic 1's are represented by no pulses and 0's are represented by pulses. The following example shows sample quantities in both logics and the pulse patterns

Quantity	Normal	Dual
A or 0	000000	111111
B or 1	000001	111110
C or 2	000010	111101
D or 3	000011	111100
62	111110	000001
63	111111	000000

Pulse Patterns



Any character or number not exceeding 63 can be represented on a 6 microsecond cycle and those quantities ranging from 64 through 4095 can be represented in the same time cycle through the use of an additional circuit. Although five binary bits are sufficient to represent alphabetic

characters, some units require six microseconds to process or operate on one character, therefore, a cycle of six microseconds has been chosen as a basic time cycle The six time positions in this cycle are referred to as T_1, T_2, T_3, T_4, T_5 and T_6 in ascending order with respect to time. In a 6-bit quantity or character, the six pulse positions are referred to as P_1, P_2, P_3, P_4, P_5 and P_6 in ascending order with respect to the power of 2. These two terminologies are not to be confused The pulses are packets of energy which travel through the circuits with a finite speed and they do not always appear at an observation point in phase with the respective time positions For example, a bus schedule represents the times at which a bus may be observed at indicated points along the bus route. An analogous concept is used to designate pulse schedules in the circuits operating in a serial mode

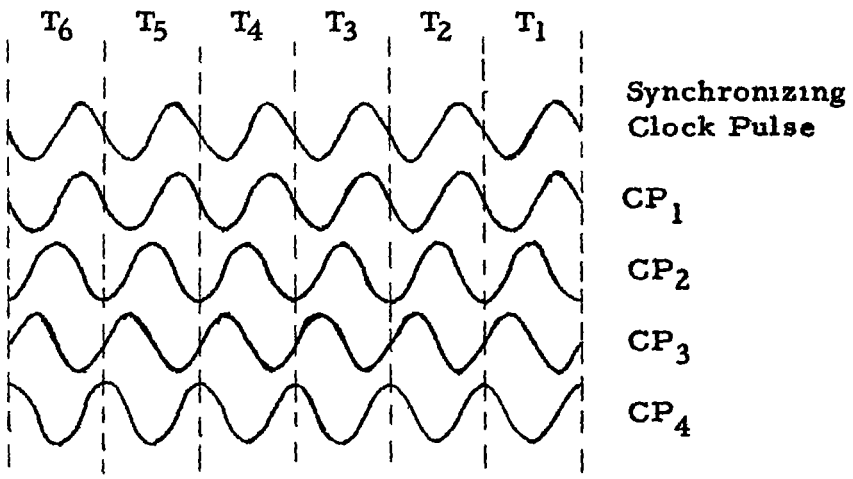
IV Circuitry and Timing

At present the circuit elements employed are of the dynamic type operating at a 1 mc/s pulse repetition frequency These circuits utilize crystal diodes for gating and switching, vacuum tubes for amplifiers and pulse regeneration, pulse transformers for a-c coupling, and delay lines for storage and time positioning elements

In order to synchronize all parts of a machine two types of timing are necessary one for microsecond timing and one for cycle timing.

A. Microsecond Timing

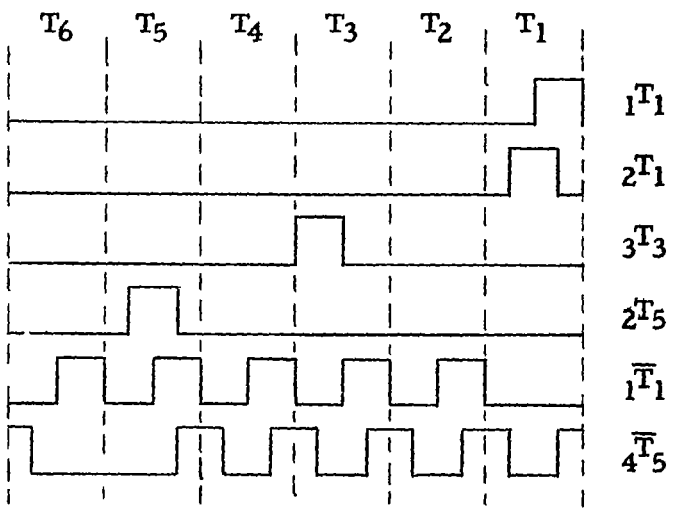
For the microsecond timing a 1 mc/s sine wave clock pulse is distributed to all clock pulse amplifiers which in turn generate the four phases to be used in timing the circuit gates Their relationship is thus



B. Cycle Timing

Provision for cycle timing and basic control for several units is made in the form of T pulses, $\overline{T}$ pulses and fixed pulse patterns. A T pulse is defined as one pulse occurring at a prescribed time position in the 6 microsecond cycle There are 24 of these T pulses identified as ${}_1T_1$, ${}_2T_1$, ${}_3T_1$, ${}_4T_1$, ${}_1T_2$, ${}_2T_2$, ${}_3T_2$, ... ${}_3T_6$, and ${}_4T_6$ The subscript on the left of the T indicates the phase of clock pulse used to generate the pulse and the subscript on the right designates the time position. A $\overline{T}$ pulse may be defined as a single blank occurring at a prescribed time position while a pulse occurs in each of the other five time positions There are 24 of these $\overline{T}$ pulses identified as ${}_1\overline{T}_1$, ${}_2\overline{T}_1$, ${}_3\overline{T}_1$, ${}_4\overline{T}_1$, ${}_1\overline{T}_2$, ${}_2\overline{T}_2$, . ${}_3\overline{T}_6$, and ${}_4\overline{T}_6$ The subscript on the left of the $\overline{T}$ indicates the phase of clock pulse used to generate the five pulses present and the subscript on the right designates the time position of the blank All possible T and $\overline{T}$ pulses are generated because it was, and still is, impossible to predict which ones will be used but the fact that they are all available, whether used or not, certainly simplifies test setups.

A fixed pulse pattern may be defined as a pattern of pulses and blanks which is repeated every cycle and remains unchanged from cycle to cycle Out of a possible 32 unique 5-bit patterns, two (00000 and 11111) can be represented by d-c voltages, five (00001, 00010, 00100, 01000 and 10000) can be represented by T pulses, and five (11110, 11101, 11011, 10111 and 01111) can be represented by $\overline{T}$ pulses All 32 patterns are needed to designate rotor output points as described in chapter 6, The Adder-Selector (AS), so the remaining 20 are generated on a pattern generator chassis The following sketch shows examples of T pulses and $\overline{T}$ pulses.



• An effort has been made to standardize unit input and output timing This standard was arbitrarily chosen as P_1 at ${}_1T_1$ which means that the first pulse position of a character, or number, coincides with ${}_1T_1$ time This simplifies the problem of tying units together

V Chassis

Based on optimum arrangements of functional circuits and their probable usage, a rather large standard plug-in chassis design has been chosen which measures approximately 17 inches high, 25 inches long, 3 inches wide, and weighs around 25 pounds filled Two plugs, each with 36 connections, are located on the back of the chassis Provision is made for 24 electron tubes on the chassis front with capacity on the side panels for the associated circuitry up to a maximum of 39 components and 8 microseconds of delay lines or 18 components and 10 microseconds of delay lines per tube The self-contained filament transformer simplifies the problem of filament power distribution This size chassis appears to be about the desirable size since it has capacity for accommodating one complete Adder-Selector, one Substitution Unit, four Mod-Counters, four Mod-Adders, the 24 T generators or the 24 $\overline{T}$ generators

VI Cabinetry

Three types of cabinetry are contemplated for housing the DERVISH chassis The first is a sort of a laboratory test set up variety of which there are two sizes, 6 chassis capacity and 10 chassis capacity Each is equipped with its own clock pulse amplifiers and a blower for cooling by room air but is dependent upon an external power supply These cabinets are designed primarily for testing individual chassis or very small groups of chassis

The second type is more of a breadboard assembly type of cabinet capable of accommodating 24 chassis It is also equipped with clock pulse amplifiers and cooling blower but is dependent upon external power supplies It's primary purpose is to permit the testing and demonstration of moderate sized assemblies or groups of chassis Inter-chassis connections are made in the form of soldered wires on the plugs on the back of the cabinet.

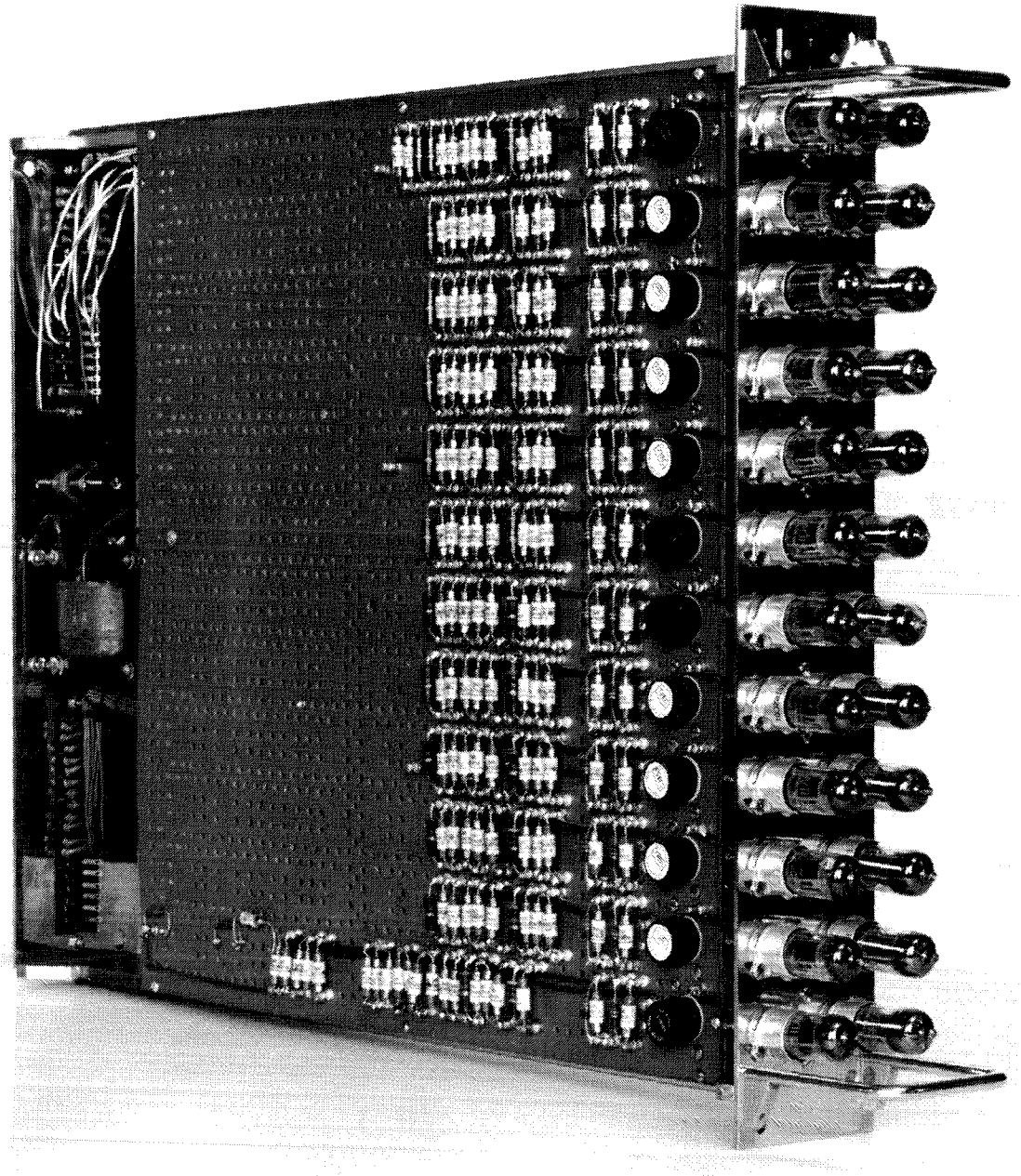
The third type is a complete self-contained cabinet system designed for operational use It is to be complete with power supplies, heat exchanger and cooling system, capacity for 72 DERVISH chassis, and an optional manual control console Inter-chassis connections are to be plug-in wires which will permit relatively rapid dismantling of one assembly and setting up of a new one Multiple cabinet systems are contemplated as being possible for very large problems

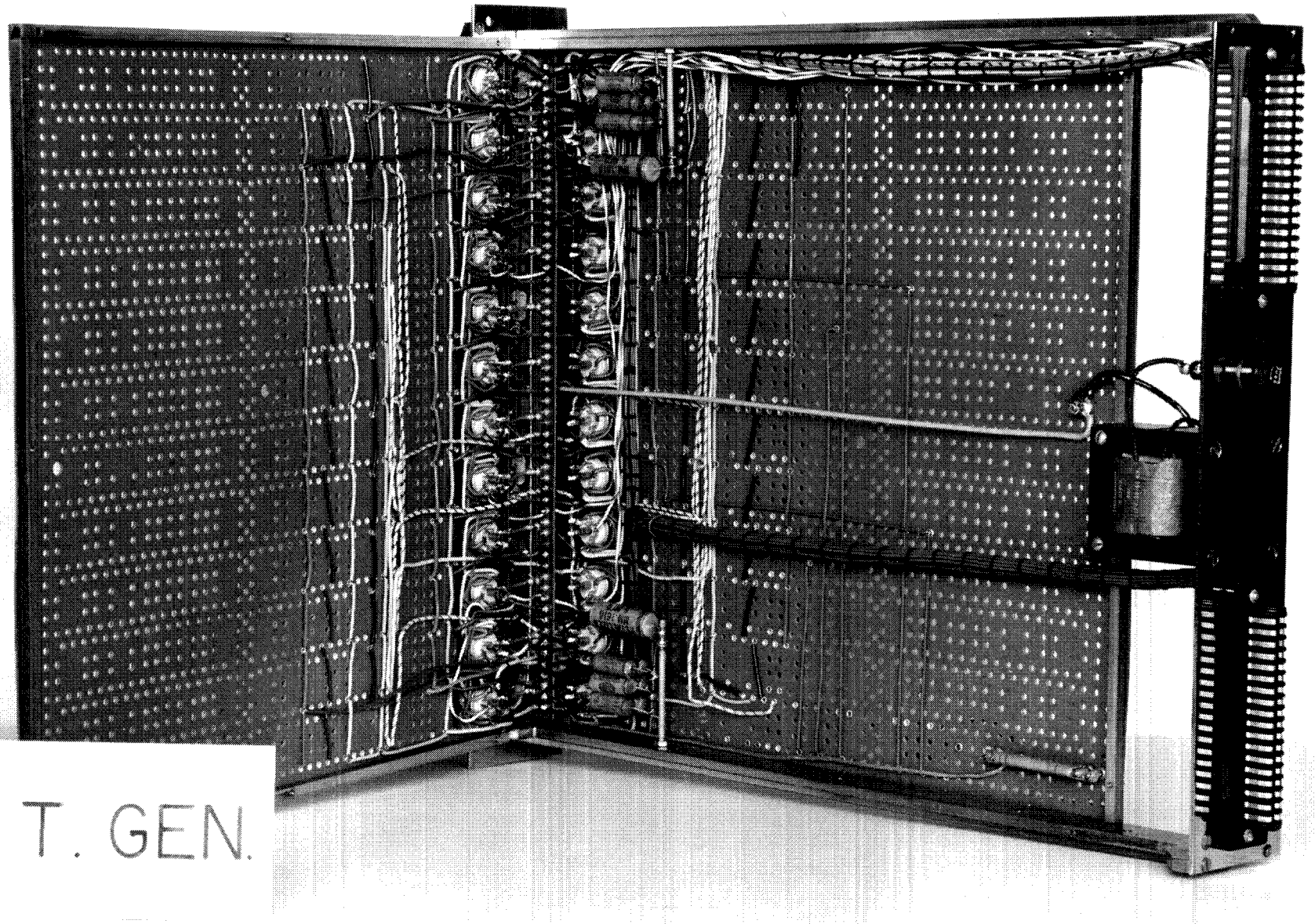
VII Future Work

Although the work on DERVISH during 1952 and 1953 was concerned mainly with units operating at a 1 mc/s pulse repetition rate which handled data in serial form, one model of an Adder-Selector (rotor) was constructed to operate in the parallel mode at a 1 mc/s rate. This represents an effective speed increase by a factor of 6 This is to be pursued further with respect to other units provided an indicated need warrants it

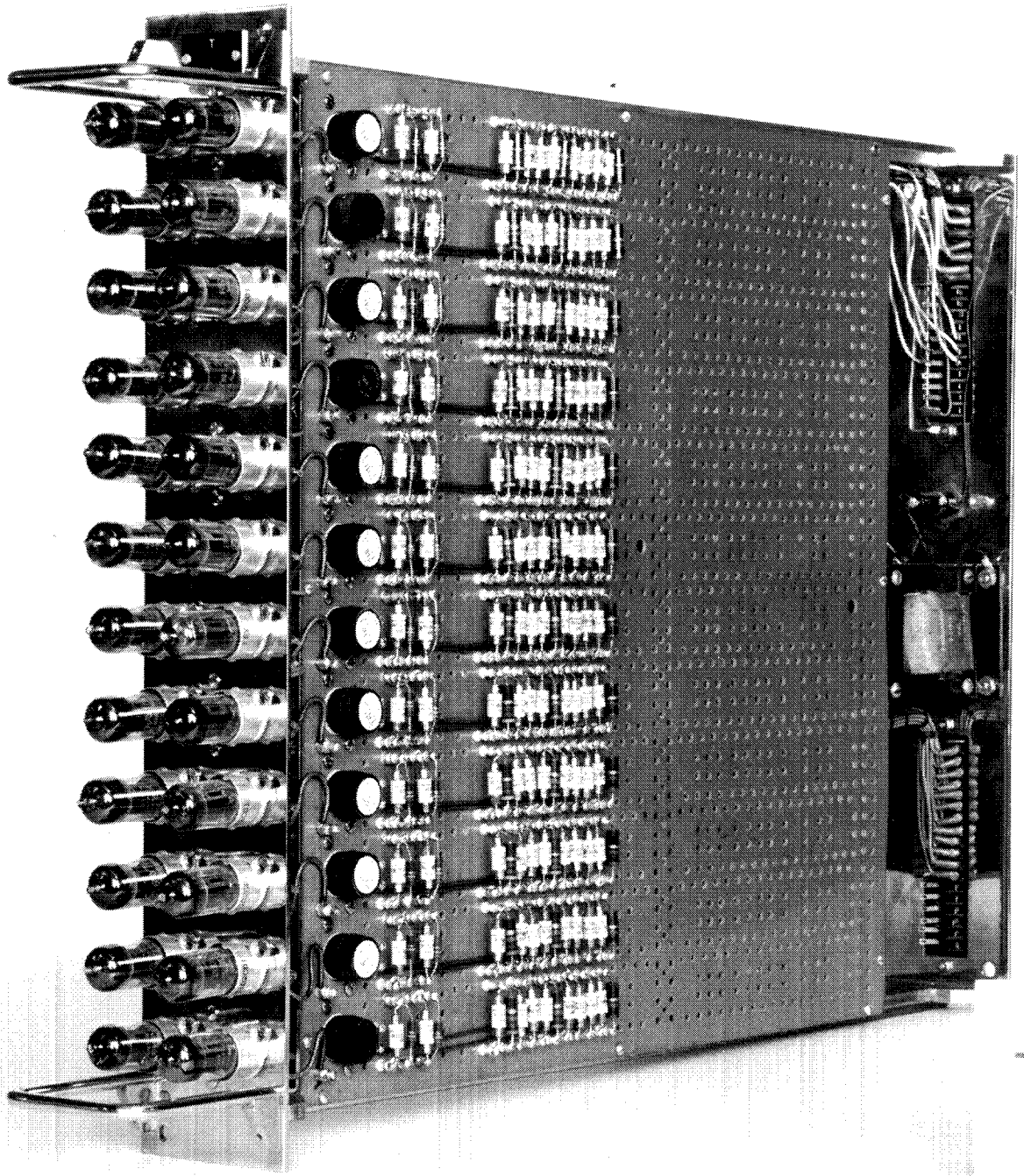
There is the possibility of increasing the pulse repetition rate to 3 or 4 mc/s or higher in order to achieve greater overall speed and yet utilize the practical aspects of serial operation New circuit techniques, developments of components such as transistors, magnetic elements and ferroelectric materials (barium titanate) may well have a bearing on the direction of future effort and are not to be overlooked

In the immediate future the main emphasis is to be placed on the construction of a sufficient quantity of units to permit assembly of some demonstrational and operational equipment utilizing the techniques now considered engineeringly sound Operational requirements will dictate the extent to which this is carried before higher speeds and parallel operation are more actively exploited



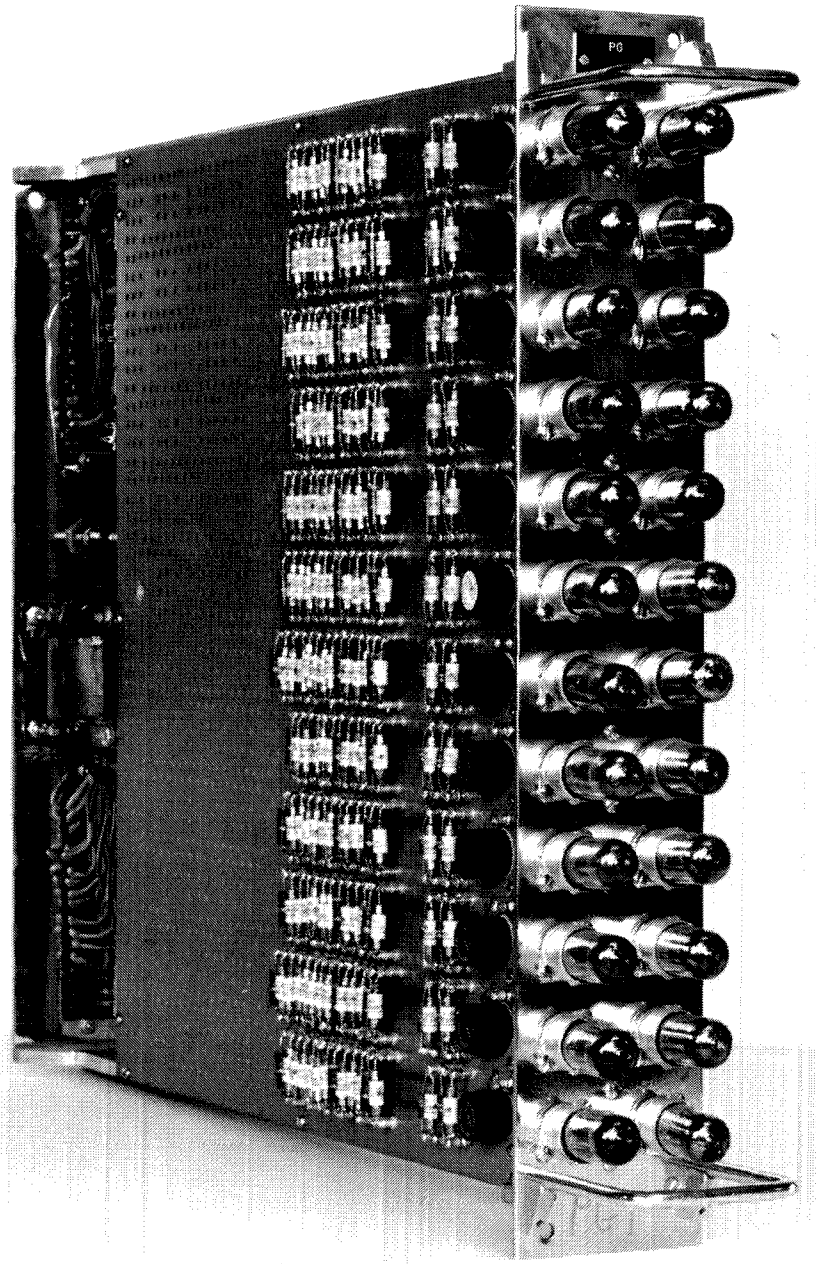


REF ID:A71743



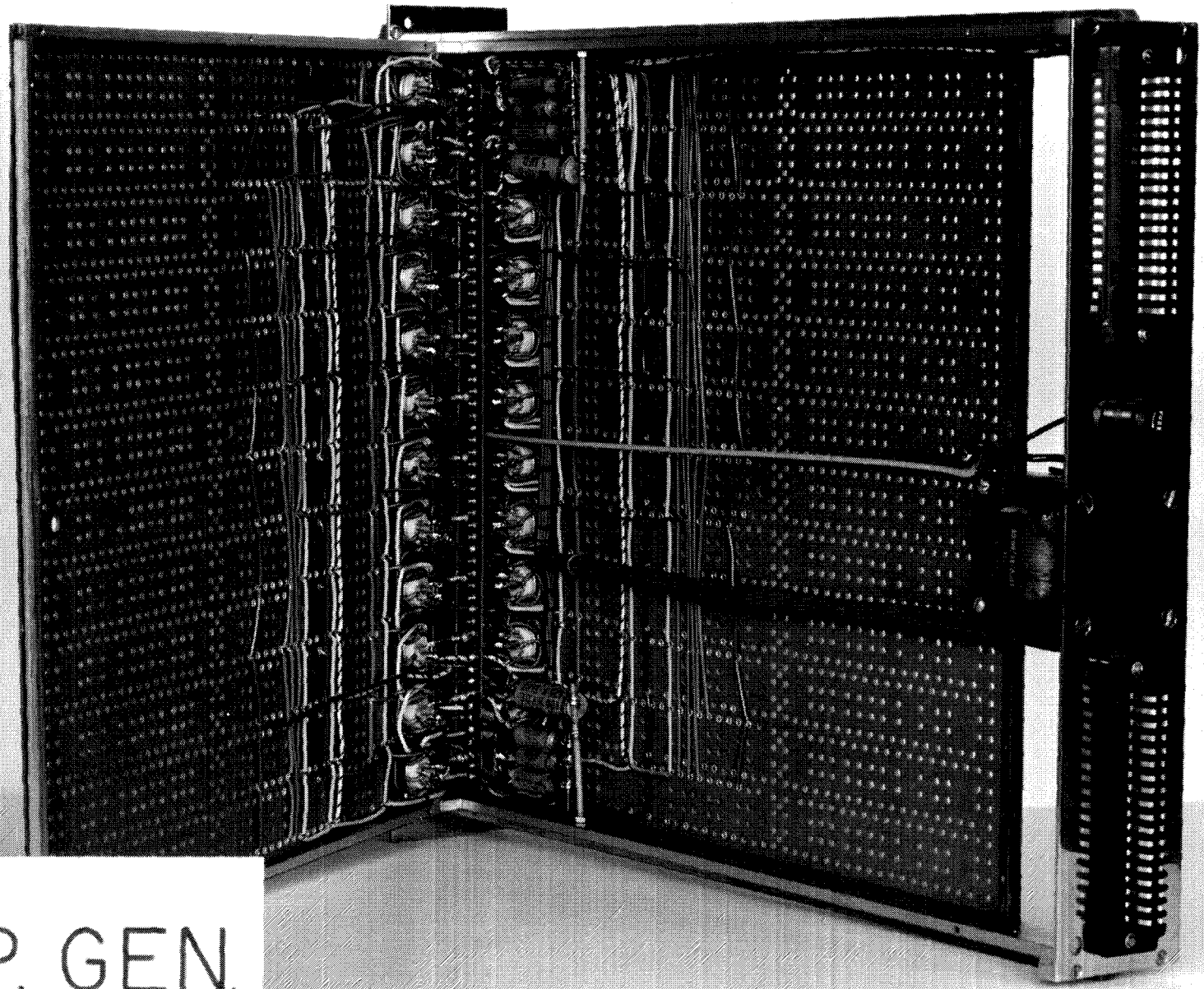
T. GEN.

REF ID:A71743



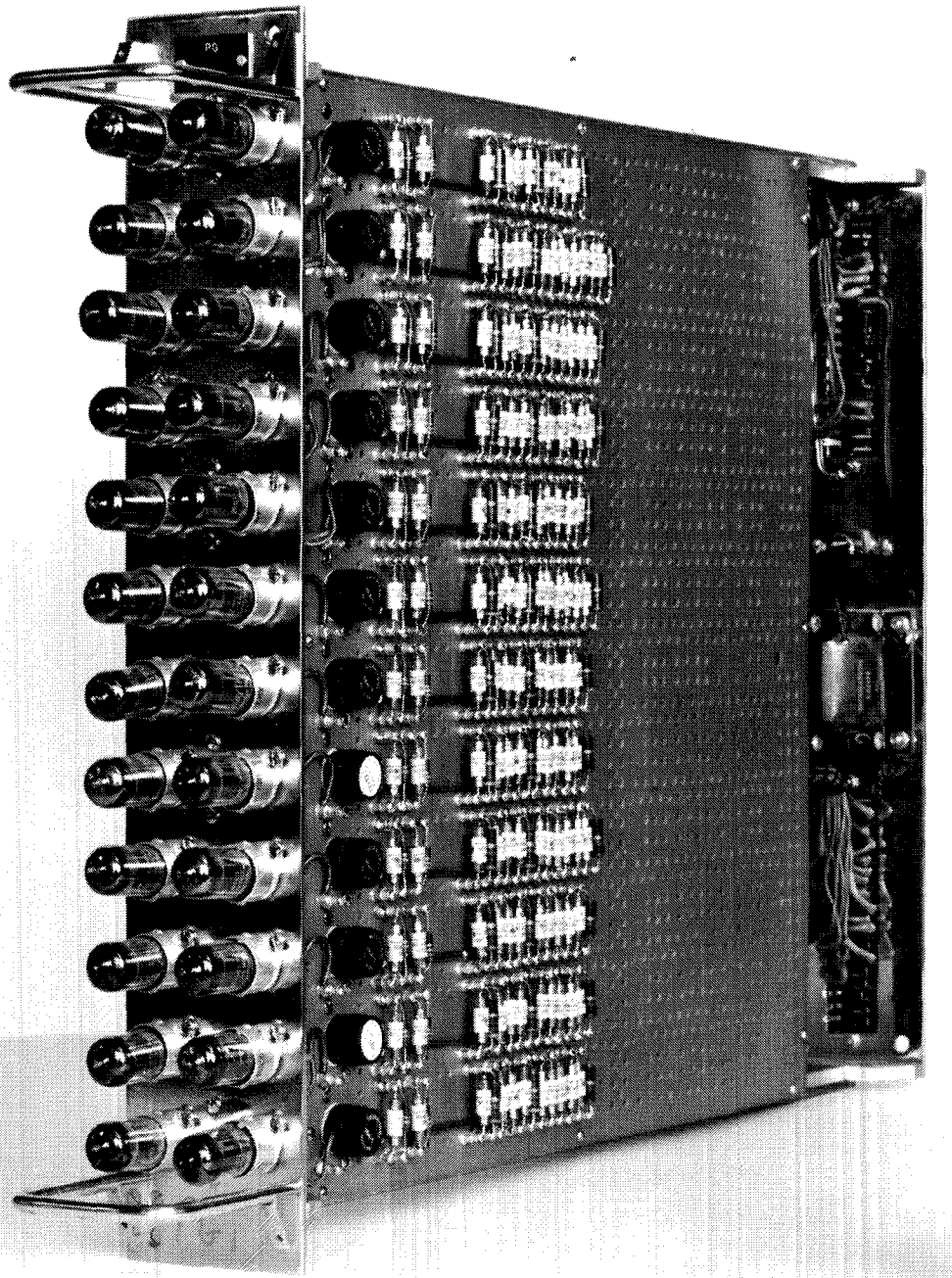
P. GEN.

REF ID:A71743



P. GEN.

REF ID:A71743



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CHAPTER 2

DEFINITIONS, SYMBOLS AND GATES

I. Scope

The purpose and scope of this chapter is to define the terms and symbols used in the following chapters and to show the component values and structures of gates used on the logical diagrams Although a number of these may appear to be rather abstract or common in some instances, it is felt that this "dictionary" should include most of the very basic terms as well as those peculiar to the type circuitry actually employed

II. Definitions

Accumulator - A device which stores a number, or quantity, and upon reception of a new number, or quantity, adds it to the previous contents and stores the sum

Adder - A device which can form the sum of two or more numbers, or quantities, impressed upon it

"AND" Gate - A circuit having an output and a multiplicity of inputs so designed that the output is energized when and only when a certain prescribed set of input conditions are met

Binary Digit (Bit) - A digit of a binary number

Binary Number - A number of the binary system which uses two symbols (usually denoted by "0" and "1") and has 2 as its base This is analogous to a decimal number of the decimal system which uses 10 symbols ("0, 1, 2, - 9") and the base 10

Borrow - (1) A condition occurring in subtraction when the difference (minuend minus the subtrahend) of two digits in the same column is negative (2) The digit to be extracted from the next column of the minuend (3) The action of extracting it

Buffer - An isolating circuit used to avoid reaction of a driven circuit upon the corresponding driving circuit

Carry - (1) A condition occurring in addition when the sum of two digits in the same column equals or exceeds the base of the number system in use (2) The digit to be forwarded to the next column (3) The action of forwarding it

Character - A letter, or symbol, of an alphabet It may be represented by a specific binary number

Character Cycle - The time required for the transmission of one character, including the space between characters

Clocked - Characteristic, or property, of having been timed with a reference timing signal

Clock Pulse - A primary timing signal with which circuits are synchronized

Complement - A number whose representation is derived from the finite positional notation of another by one of the following rules (a) True Complement (twos complement) - Subtract each digit from the radix less one, then add one to the least significant digit, executing any carries required (b) (Radix - 1)'s Complement (ones complement) - Subtract each digit from the radix less one

Counter - A device capable of changing from one to the next of a sequence of distinguishable states upon each receipt of a discrete input signal

Cycle - An interval of time in which is completed one round of events, or phenomena, that recur regularly and in the same sequence

Delay Line - A circuit component wherein a finite time is required for a pulse of electrical energy to traverse its physical length

Diode - A non-linear circuit component which exhibits a high resistance to current flow in one direction and a low resistance in the opposite direction

Enabler - Any input to an "AND" gate that is actuated by positive going signals, the presence of such a signal being required for the "AND" gate to operate.

Dynamic Flip-Flop - An electronic circuit which has two operational states and ordinarily two types of input signals (turn ON and turn OFF) Its output is a continuous stream of pulses when ON and no pulses when OFF

Inhibitor - Any input to an "AND" gate that is actuated by negative going signals, the absence of such a signal being required for the "AND" gate to operate

Memory - A device into which information may be introduced and then extracted at a later time

Number - A representation of an abstract mathematical entity defined by the rules governing the relations and operations to which it is susceptible such as a binary number, or a decimal number, or a sequence of pulses.

"OR" Gate - A circuit having an output and one or more inputs so designed that the output is energized whenever one or more inputs are energized Thus an "OR" gate is frequently considered as a buffer or isolating circuit

Preset - Commonly refers to a condition in a counter whereby the counter's beginning point is established at some value other than zero

Pulse - A signal of electrical energy normally of short duration

Pulse Timing	- A system of designating a time schedule of specified pulse positions
Radix (or Base)	- The integer of whose successive powers the digits of a number are the coefficients
Read	- To extract information
Reset	- (1) The action of an electronic circuit being returned to its normal initial condition (2) The control function which effects this return
Rotor	- A disc designed to rotate within an electrical cipher machine with a set of input contacts and a set of output contacts connected by any prearranged scheme
Selector	- A device capable of choosing any one of a multiplicity of items In DERVISH, it is an electronic switching circuit capable of choosing for an output any one of a number of inputs
Shift	- Displacement of an ordered set of digits (bits) one or more columns to the right or left
Stage	- Commonly refers to one set of electron tube elements and their associated circuit components
Staticize	- To take one or more digits (bits) normally moving through a series of circuit stages and store them in individual storage elements
Storage Loop	- A specific type of memory device normally of delay lines with its ends connected thereby allowing its content of digits to circulate within it on a cyclic basis
T Pulse	- A single pulse occurring at a prescribed time position of a repetitive time cycle
$\overline{T}$ Pulse	- A single blank, or no pulse, occurring at a precribed time position in a repetitive cycle while pulses occur at all other time positions

Timing Numbers - A set of numbers used to define the corners of the utilized trapezoidal portion of an electrical pulse

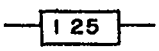
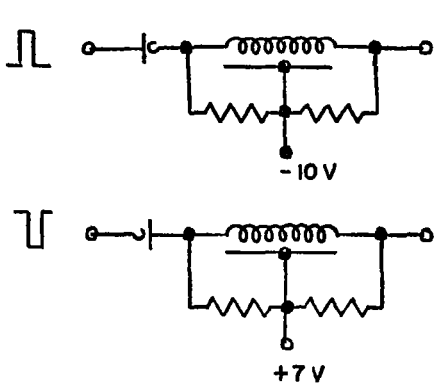
Tolerance - An indication (normally by a set of numbers) of the allowable deviation of pulses which are driving a gate and yet maintain reliable operation of that gate

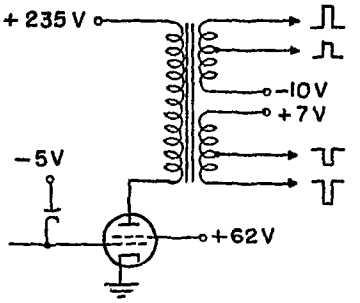
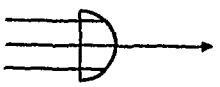
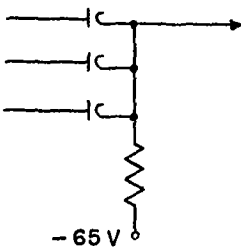
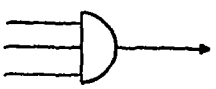
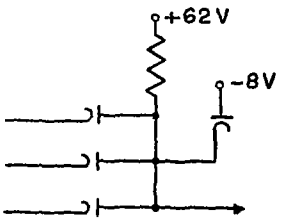
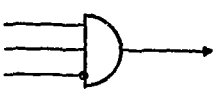
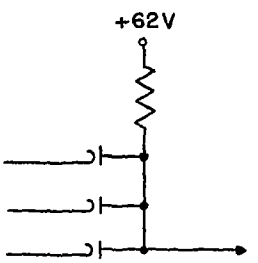
Translator - A device capable of accepting information in one number system or code and changing that information into another number system or code "Encoder" is frequently used to identify a device capable of translating information in one number system to a machine code and "decoder" to identify a device capable of translating information in a machine code to a number system

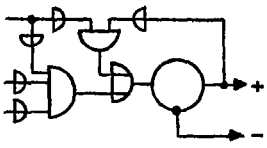
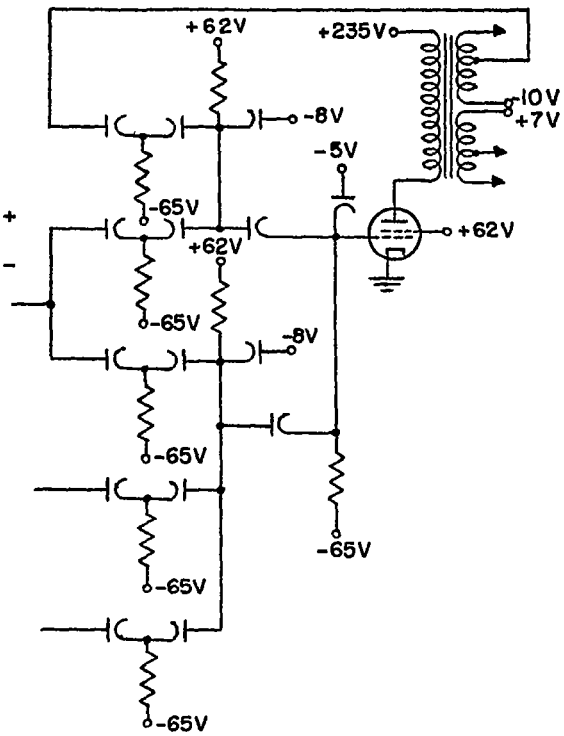
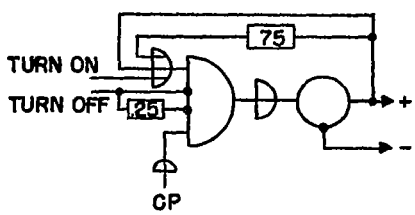
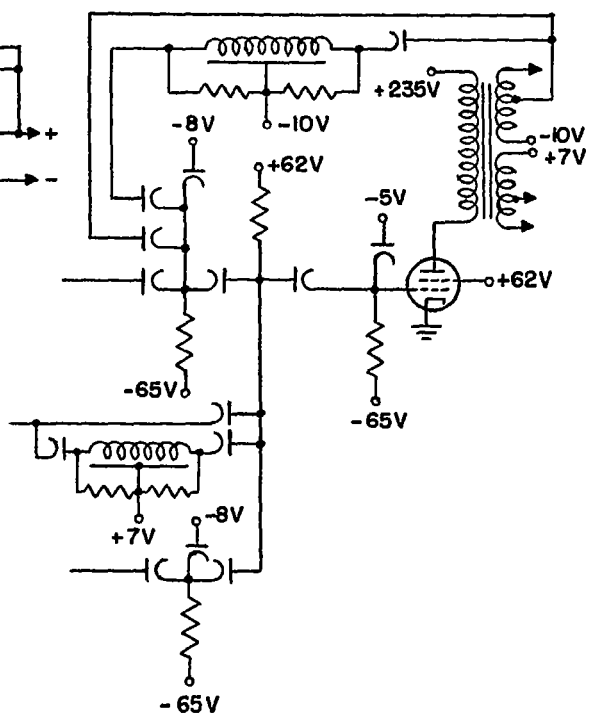
Write - Insert Information

III Symbols

The set of symbols adopted in DERVISH is normally the same as that used with SEAC by the National Bureau of Standards and with ABNER by NSA-35 No set of symbols has been standardized for comparable circuit or logical diagrams as yet in the electronics field since the recent rapid growth of the fields of computation and data processing has produced a wide variety of symbols and notations

Item	Logical symbol	Component diagram
Delay line		

Item	Logical symbol	Component diagram
Tube		
"OR" gate		
"AND" gate		
"AND" gate (with inhibitor)		

Item	Logical symbol	Component diagram
Normal Gating Arrangement		
Flip-Flop		

IV Timing Numbers and Gate Tolerances

A. Timing Numbers

In dynamic circuitry it is very important that pulses be well defined with respect to time in order that circuit components affecting pulse shape and delay may be properly chosen to give reliable operation at every point in the circuit especially where a number of signals are combined in some manner to perform a logical function A system of timing numbers has been adopted which provides a way of describing the shape and time location of the utilizable portion of any pulse at any point in a circuit The portion of a pulse that is really utilized is that portion lying between -5 V. d-c and +2 V. d-c The timing numbers designate the times within a microsecond period when these two voltage levels intersect the leading and trailing edges of a pulse and this is represented by the expression

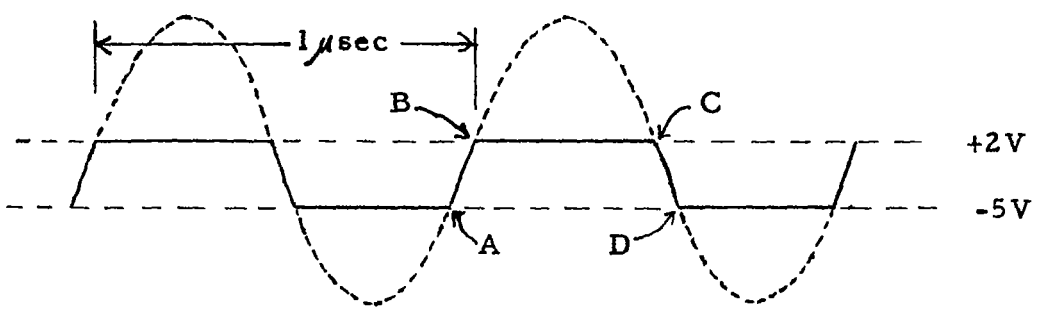
$$\begin{array}{|c|c|}\hline B & C \\ \hline A & D \\ \hline \end{array}$$

A, B, C and D are expressed in hundredthsof a microsecond where A indicates the time when the leading edge or rising voltage is -5 V , B indicates the time when the rising voltage is +2 V , C indicates the time when the trailing edge or falling voltage is +2 V , and D indicates the time the trailing edge is down to -5 V The amount of pulse above the +2 volt level is not indicated normally but is +4 V or higher which gives a considerable amplitude margin of safety.

The clock pulses are the basic timing and synchronizing signals The first one was arbitrarily chosen and the others fall in line thusly

CP_1 $\begin{array}{|c|c|}\hline 25 & 72 \\ \hline 20 & 77 \\ \hline \end{array}$ CP_2. $\begin{array}{|c|c|}\hline 50 & 97 \\ \hline 45 & 102 \\ \hline \end{array}$ CP_3 $\begin{array}{|c|c|}\hline 75 & 122 \\ \hline 70 & 127 \\ \hline \end{array}$ CP_4 $\begin{array}{|c|c|}\hline 100 & 147 \\ \hline 95 & 152 \\ \hline \end{array}$

The following sketch shows the timing number points and the utilized trapezoidal portion of a clock pulse.

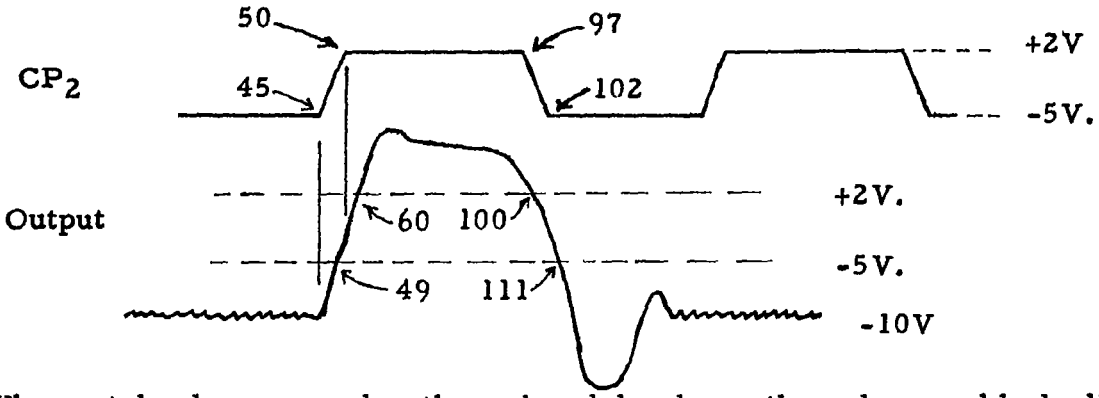


A certain amount of delay is incurred when a clocked signal passes through a gate structure, tube and transformer The aggregate delay for all these components for all conditions of pulse (first through Nth) has been combined into one set of numbers thus

$$\begin{array}{c|c} 10 & 3 \\ \hline 4 & 9 \end{array}$$

The numbers 4, 10, 3 and 9 indicate the maximum delay under any condition for points A, B, C and D in going through one stage Therefore, the output pulse from a stage clocked with CP_2 is

$$\begin{array}{c|c} 50 & 97 \\ \hline 45 & 102 \end{array} + \begin{array}{c|c} 10 & 3 \\ \hline 4 & 9 \end{array} = \begin{array}{c|c} 60 & 100 \\ \hline 49 & 111 \end{array}$$



When a tube drives a pulse through a delay line, the pulse would ideally be shifted in time but for practical considerations it is also distorted due to attenuation which is a function of the length of line The pulse is narrowed at the top and broadened at the bottom since the frequency band pass of the delay line is considerably below 5 Mc/s thereby seriously attenuating the harmonics in a pulse Timing numbers are modified to accomodate this distortion according to the following

0 to 0 33 μsec $\begin{array}{c|c} +1 & -1 \\ \hline -1 & +1 \end{array}$

0.34 to 0 66 μsec $\begin{array}{c|c} +2 & -2 \\ \hline -2 & +2 \end{array}$

0 67 to 0 99 μsec $\begin{array}{c|c} +3 & -3 \\ \hline -3 & +3 \end{array}$

1.00 μsec and over $\begin{array}{c|c} +5 & -5 \\ \hline -5 & +5 \end{array}$

The pulse output of a 50 microsecond delay line driven by a stage clocked with CP_1 is

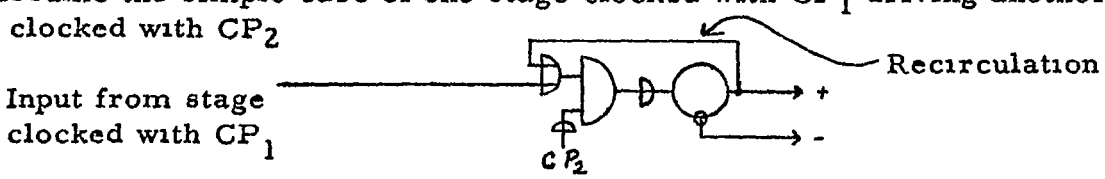
$$\begin{array}{c|c} 25 & 72 \\ \hline 20 & 77 \end{array} + \begin{array}{c|c} 10 & 3 \\ \hline 4 & 9 \end{array} + \begin{array}{c|c} 50 & 50 \\ \hline 50 & 50 \end{array} + \begin{array}{c|c} +2 & -2 \\ \hline -2 & +2 \end{array} = \begin{array}{c|c} 87 & 123 \\ \hline 72 & 138 \end{array}$$

B. Gate Tolerances

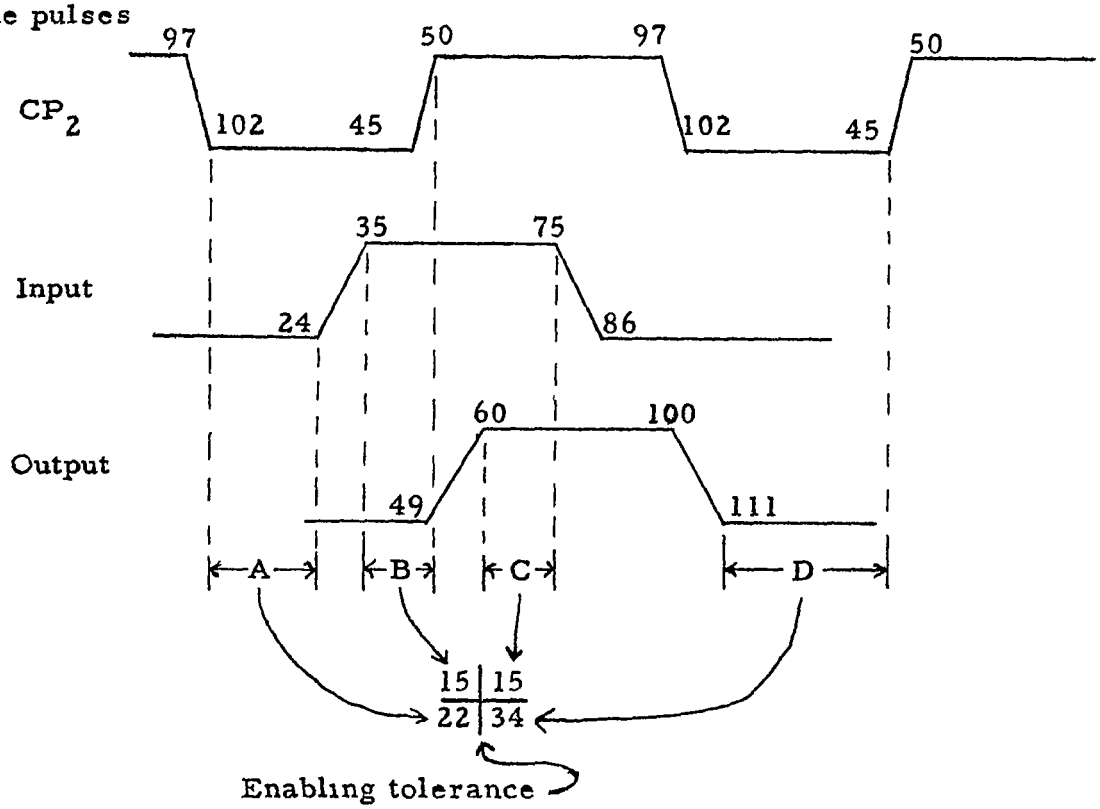
In the normal sense tolerance is understood to mean a specified allowance for error in weighing, measuring, etc., or variations from the standard or given dimensions, weight, or the like In the sense as applied to dynamic circuitry, it indicates the maximum allowable deviation a pulse or set of pulses may vary in shape or time position without affecting the reliable operation of a gate. This usually applies to the "AND" gate of a stage and is calculated for both enabling and inhibiting conditions

(1) Enabling Tolerance

Assume the simple case of one stage clocked with CP_1 driving another stage clocked with CP_2



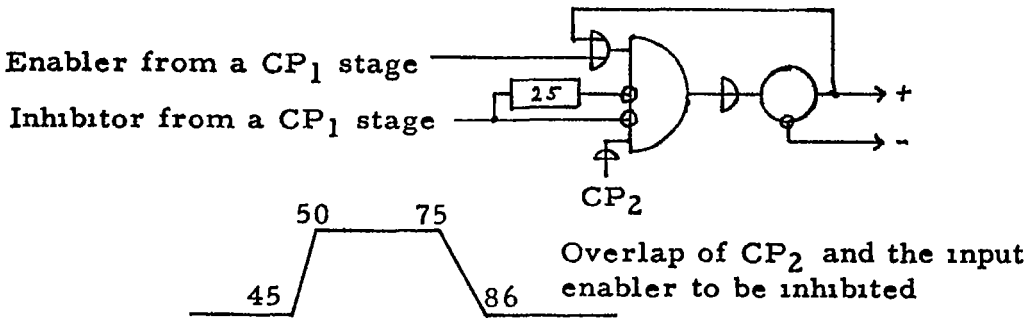
The recirculation is used as a method of maintaining an input pulse for the full duration of the clock pulse in order to get a fully regenerated and reshaped output pulse The following sketch shows the time relationship of the pulses



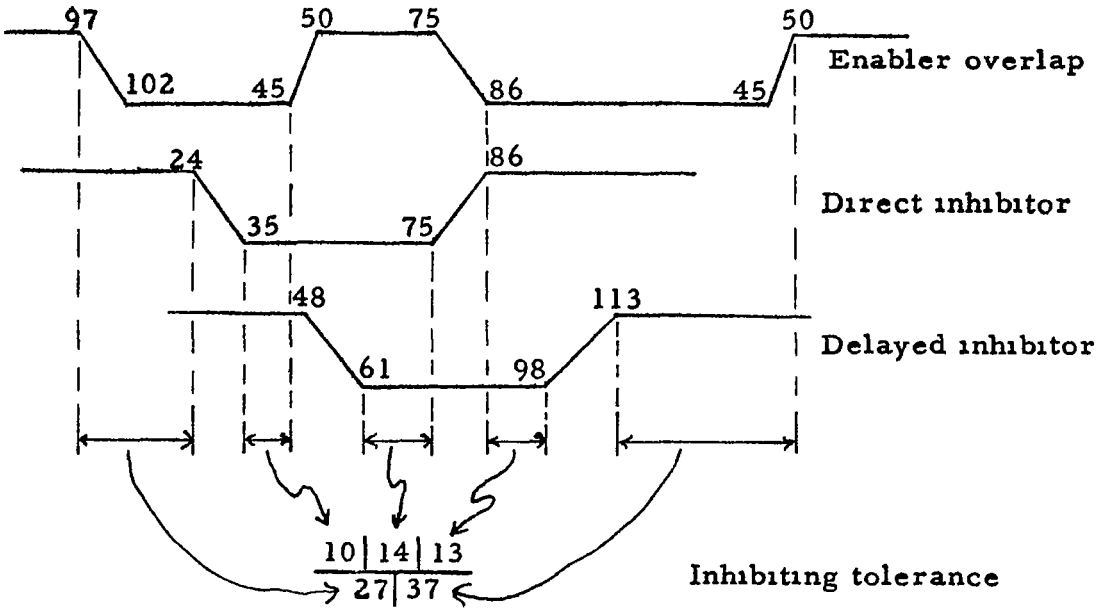
The ideal case is to get the B and C tolerances equal In the system where four phases of clock pulse are employed this is quite easily achieved When more than one input pulse is used, the A tolerance is determined by the input having the earliest A point, the B tolerance is determined by the input having the latest B point, the C tolerance by the input having the earliest C point, and the D tolerance by the output pulse D point

(2) Inhibiting Tolerance

When an inhibitor is used, it must be remembered that an "AND" gate can operate only when all inputs are enabled, therefore, to inhibit an "AND" gate the inhibitor pulse needs to be wide enough to prevent gate action during the composite overlap of all the inputs Take the following simple case with one enabler and one clock pulse to be inhibited.

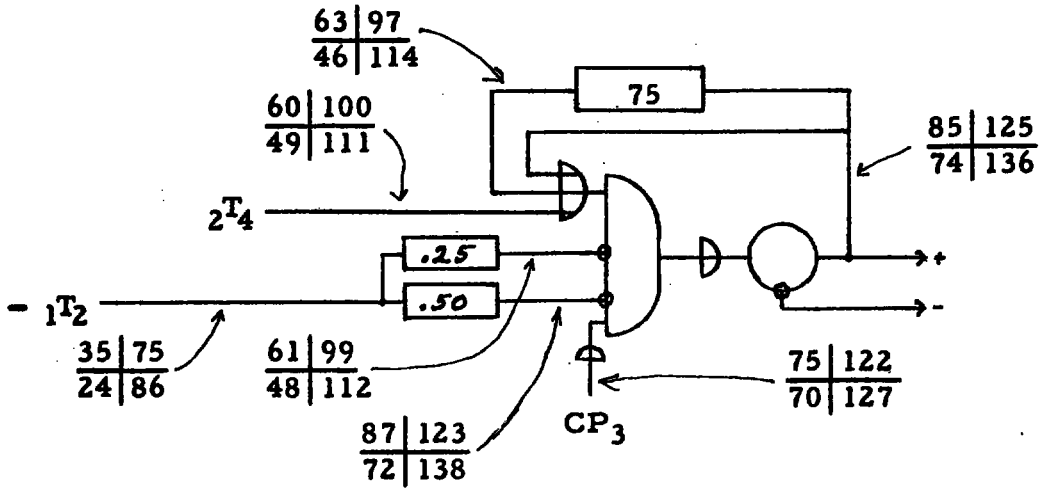


The inhibitor and enabler time relationship is as follows·



It can be seen that the inhibitor pulse is not wide enough to completely prevent gate action, therefore, it is effectively broadened by a .25 microsecond delay line to provide inhibition over the entire overlap period of the enablers plus a margin of safety.

The following example shows a simple arrangement of a flip-flop with timing numbers for all the leads and the "AND" gate tolerances:

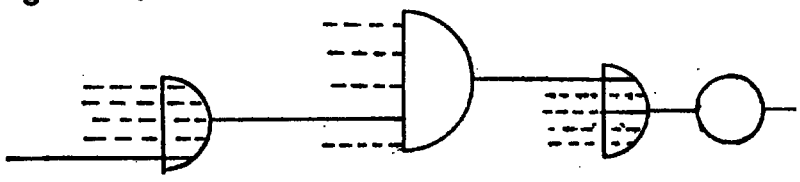


$$\text{Enabling tolerance} = \frac{(75-63)\,|\,(97-85)}{(46-27)\,|\,(70-36)} = \frac{12\,|\,12}{19\,|\,34}$$

$$\text{Inhibiting tolerance} = \frac{(70-61)\,|\,(99-87)\,|\,(23-14)}{(48-22)\,|\,(75-38)} = \frac{9\,|\,12\,|\,9}{26\,|\,37}$$

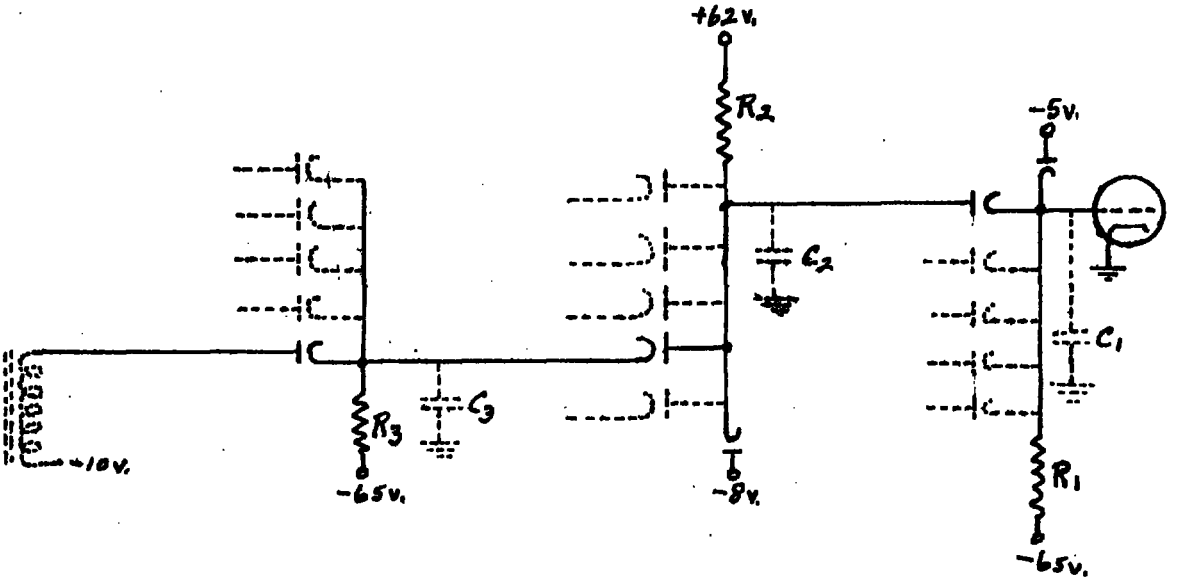
V. Gate Resistor Calculations

Gating circuits may take any of a large number of forms depending on function and type of circuit components. An "OR-AND-OR" arrangement has been adopted as normal practice in dynamic circuitry for a gating structure associated with a tube. The following example shows this "OR-AND-OR" arrangement:



"OR" "AND" "OR"

This arrangement not only allows for a wide variety of ways to combine signals but also isolates all input signals from each other and the tube grid. The following sketch shows the component arrangement of the "OR-AND-OR" structure:



The resistor values are calculated to provide pulse rise and fall times of 0.1 microsecond or less when up to five inputs are connected into each resistor. The voltage excursions on the grid are between -5.5 V. and +2 V. with the -5.5 V. limit provided by a bumper diode with a half volt drop to -5 V. and the +2 V. limit provided by grid current although in practice this does go a little higher. R_1 is calculated first. It must supply sufficient current to discharge C_1 from +2 V. to -5.5 V. in 0.1 microsecond. C_1 consists of 9 mmfd tube input capacitance plus 6 mmfd for wiring capacitances making a total of 15 mmfd. The average rate of discharge of C_1 is therefore 75 volts per microsecond. The actual shape of the curve is not linear but rather exponential whose slop at any point is: $\frac{de}{dt} = \frac{E}{R_1 C_1} \epsilon^{-\frac{t}{R_1 C_1}}$ where e is the voltage across R_1 at time t, and E is the initial voltage across R_1. But $e = E \epsilon^{-\frac{t}{R_1 C_1}}$, therefore, $\frac{de}{dt} = \frac{e}{R_1 C_1}$. The steepest part of the curve is at the +2 V. level where C_1 is just starting to discharge so a conservative method is to choose the -5.5 V. level as having a 75 volt/μsec slope at which point

$$\frac{de}{dt} = \frac{59.5}{R_1 C_1}$$

$$\frac{75}{10^{-6}} = \frac{59.5}{R_1 \times 15 \times 10^{-12}}$$

$$R_1 = \frac{59.5 \times 10^6}{15 \times 75}$$

$$= 52,888 \text{ ohms}$$

Allowing for 10% tolerance $R_1 = 52,888 \times \frac{10}{11} = 48,080$

R_1 is then chosen as 47K.

The formula using voltage doesn't apply easily for calculating R_2 but the formula for current is more easily used. R_1 can also be calculated from the current flow.

$$i = \frac{dq}{dt}$$

Substituting $q = Ce$ $\quad i = C \frac{de}{dt}$

This formula applies to R_1 as well as the one used above.

Current through $R_1 = \frac{15 \times 10^{-12} \times 75 \times 10^3}{10^{-6}}$

$$= 15 \times 75 \times 10^{-3}$$

$$= 1.125 \text{ ma}$$

$$R_1 = \frac{59.5}{1.125} = 52,888 \text{ ohms}$$

Allowing for 10% tolerance $R_1 = 52,888 \times \frac{10}{11} = 48,080$ ohms

Use R_1 = 47K

In calculating R_2 it is pointed out that R_2 must supply three separate currents: (1) the maximum current that can exist in R_1, (2) the current to charge C_1 and C_2, and (3) the back current for the remaining diodes connected to R_1. The charging current for C_1 and C_2 is not exactly constant but is maximum at the start and minimum at the finish. Also the diode back current is not constant but is zero at the start and a finite value at the finish. These two currents overlap in time but not when both are maximum, therefore, the assumption is made that,on the average, one half of the diode back current is concurrent with the charge current. C_2 = 5 mmfd and the

diode back resistance is allowed to be as low as 50K. Allowing 0.5 volts drop across the diode connecting R_2 and R_1 the following expression applies:

$$\text{Current through } R_2 = \frac{65 + 2}{0.9\ R_1} + \frac{(C_1 + C_2)75}{10^{-6}} + \frac{1/2 \times 10}{1/5 \times 50}$$

$$= \frac{67}{42.3} + \frac{20 \times 10^{-12} \times 75 \times 10^{3}}{10^{-6}} + \frac{5}{10}$$

$$= 1.584 + 1.500 + .500$$

$$= 3.584 \text{ ma}$$

$$R_2 = \frac{59.5}{3.584} = 16{,}602 \text{ ohms}$$

Allowing for 10% tolerance $R_2 = 16{,}602 \times \frac{10}{11} = 15{,}093$

Use $R_2 = 15K$

R_3 must also supply three separate currents: (1) the maximum current that can exist in R_2, (2) the current to discharge C_2 and C_3, and (3) the back current for the remaining diodes connected to R_2. C_3 = 5 mmfd. Allow one half volt drop across the diode connecting R_3 to R_2.

$$\text{Current through } R_3 = \frac{62 + 9}{0.9\ R_2} + \frac{(C_2 + C_3)\ 75}{10^{-6}} + \frac{1/2 \times 12}{1/5 \times 50}$$

$$= \frac{71}{13.5} + \frac{10 \times 10^{-12} \times 75 \times 10^{3}}{10^{-6}} + \frac{6}{10}$$

$$= 5.259 + 0.750 + 0.600$$

$$= 6.609 \text{ ma}$$

$$R_3 = \frac{65 - 9}{6.609} = 8{,}473 \text{ ohms}$$

Allowing for 10% tolerance $R_3 = 8{,}473 \times \frac{10}{11} = 7{,}703$ ohms

Use $R_3 = 7.5K$

There are several methods for calculating these gate resistors depending upon the assumptions made and the results vary over a rather wide range such as this:

R_1 ranges from 36K to 51K
R_2 ranges from 13K to 20K
R_3 ranges from 7.5K to 12K

In practice, however, crystal diodes have a finite back resistance which assists R_3 in discharging C_2 and C_3 and the tube grid assists R_1 in discharging C_1. It is also true that the greater the ratio of R_2 to R_1 the lower the permissible back resistance of the "AND" gate crystals.

The following tables show current values in milliamperes for the gate resistors:

For R_1 = 47K		at top of swing +2 V.	at bottom of swing -5.5 V.
51.7K	minimum	1.296	1.151
47K	design center	1.426	1.266
42.3K	maximum	1.584	1.407

For R_2 = 15K		at top of swing +2.5 V.	at bottom of swing -8.5 V.
16.5K	minimum	3.606	4.273
15K	design center	3.967	4.700
13.5K	maximum	4.407	5.222

For R_3 = 7.5K		at top of swing +6 V.	at bottom of swing -9 V.
8.25K	minimum	8.606	6.788
7.5K	design center	9.467	7.467
6.75K	maximum	10.519	8.296

CHAPTER 3

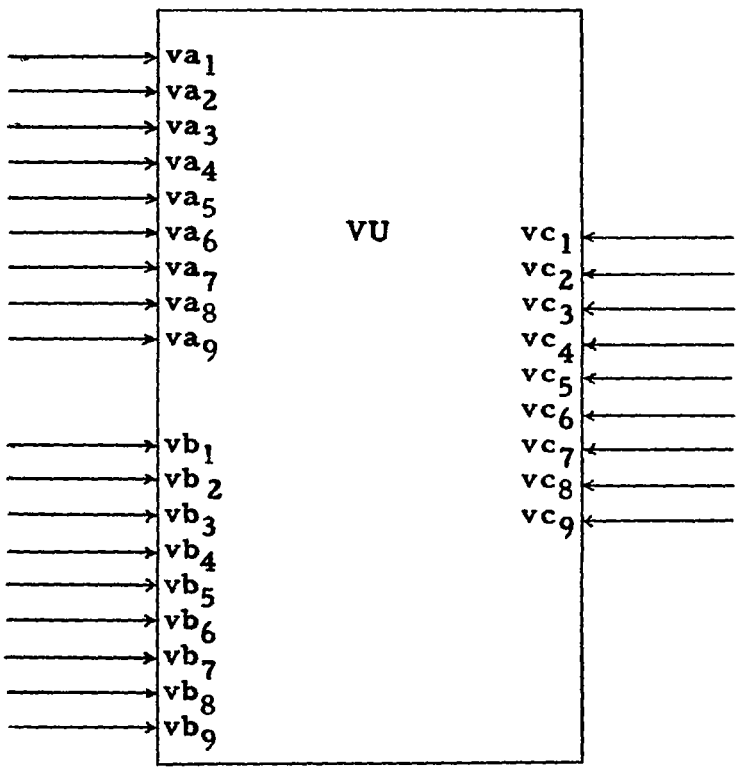
THE VISUAL UNIT (VU)

I Function

The function of the Visual Unit is to accept a 6-bit binary pattern of pulses and display it on lights along with its decimal interpretation This will fulfill the need for evaluating binary patterns of pulses quickly during both testing and operation

II Symbolic Representation

The following sketch shows how the Visual Unit may be represented in a block diagram·



The functions of the leads may be defined as follows.

va_1 to va_9 - Inputs associated with switch S_1 Each may have P_1 at any time within the range $_1T_5$ through $_1T_1$

vb_1 to vb_9 - Inputs associated with switch S_2. Each may have P_1 at any time within the range $_1T_1$ through $_1T_3$.

vc_1 to vc_9 - Inputs associated with switch S_3. Each may have P_1 at any time within the range $_1T_5$.

III. Application

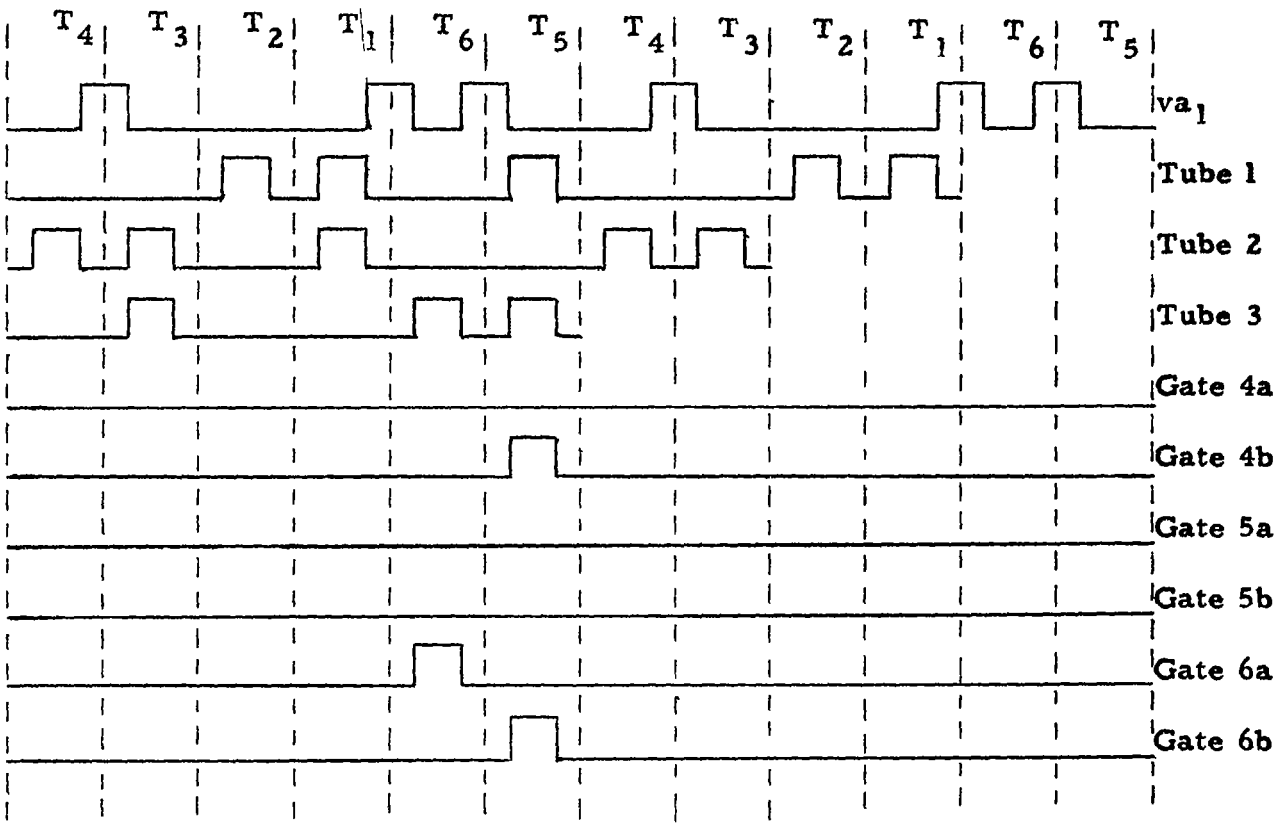
There is only one logical application for the Visual Unit. It is a means whereby a quick visual interpretation of a pattern of six pulses may be obtained directly without the aid of an oscilloscope. When built into a machine or an assembly of units, its chief purpose would be to permit an operator to display visually quantities present in counters, adders, storage units, etc. On problems where recording time is of no great significance this makes possible a quick visual recording facility without providing necessary circuitry to operate a page printer or typewriter. It has obvious advantages during system testing and trouble shooting as well.

IV. Operation

The main portion of the Visual Unit consists of a six microsecond storage loop with three input points and a translator to convert its contents to an easily readable form. The three input points are associated with the three tubes in the storage loop. At each point a 10 position 2 gang switch selects one of nine inputs or allows the loop to be closed. For example: switch S_1 associated with tube 1, is used to select inputs on lead va_1 on position 1, lead va_2 on position 2, etc. through position 9. In its zero position nothing comes in and the loop is closed for pulse circulation at that point. In order to position input patterns properly each input is supplied with places for delay lines in increments of .25 microseconds from zero up to and including 2.00 microseconds. The three tubes in the storage loop are spaced two microseconds apart in time. This in conjunction with the variable delays for each input signal makes it possible to accept a 6-bit pattern timed at any time in the six microsecond cycle. For proper operation two of the three switches must be set on their zero positions in order to insure a full six microseconds of storage for a pulse pattern entering via the third switch.

The six pulse positions of the storage loop are sampled every six microseconds and stored on six detectors each of which drive a two position relay through a triode to control the translator. One contact of each relay operates a neon light in addition.

The following sketch shows pulse patterns for the value 44 timed P_1 at ${}_4T_5$ fed in on lead va_1



The translation is done in two parts The first part consists of two 3 to 8 translators and the second part is an 8 x 8 matrix The three low order bits P_1, P_2 and P_3 operate a 3 to 8 translator tied to -65 volts and the three high order bits P_4, P_5 and P_6 operate a 3 to 8 translator tied to +62 volts The two sets of 8 outputs thus derived are used to drive the two sets of coordinates of the 8 x 8 matrix containing a neon at each intersection At the intersection where one coordinate is high from the +62 volt translator and the other coordinate is low from -65 volt translator one neon is illuminated which indicates the decimal value of the 6-bit pattern The 6-bit pattern is displayed on the set of 6 neons For example, the value 44 causes neons 32, 8 and 4 of the set of 6 neons to be illuminated and neon 44 of the set of 64 to be illuminated The relays in the Visual Unit forbid its use as a continuous monitor for patterns that are constantly changing at a rapid rate, however, it may be used as a monitor for patterns that remain constant for several seconds such as those encountered in a slow running Mod Counter

IV. Physical Characterictics

The Visual Unit is built on one chassis with an approximate circuit component requirements as follows:

Vacumm tubes:	3 type 6AN5, 3 type 12AT7
Pulse transformers:	3 plug-in ferrite type
Crystal diodes:	158 Kemtron type K-345
Delay lines:	6 sticks minimum, 60 sticks maximum
Resistors:	172
Filament transformer:	1 Thordarson type T21F12
Relays:	6 type SM5LG (Potter-Brumfield)
Neons:	70 type NE2
Switches:	3 Grayhill miniature 10 pos. 2 decks

The power consumption on the more important voltages for one chassis is approximately as follows:

	Current	Watts
+200 V.	0.18 amps	36
+62 V.	0.26 amps	16
-8 V.	-0.03 amps	-.24
-65 V.	0.39 amps	25
110 V. a.c.	.14 amps	15

The total power consumption is approximately 90 to 100 watts which represents a heat dissipation of 5 to 6 B.T.U. per minute.

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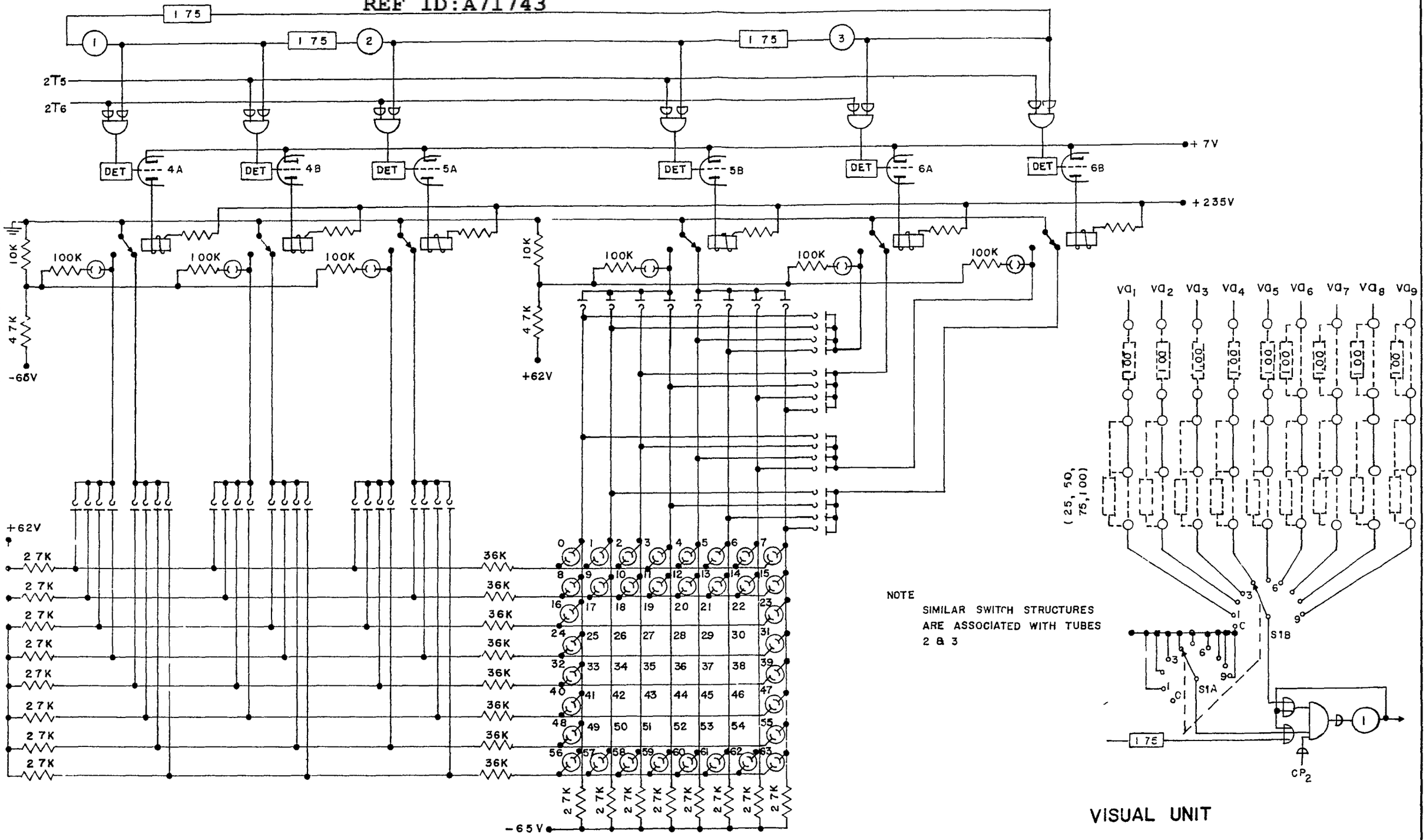
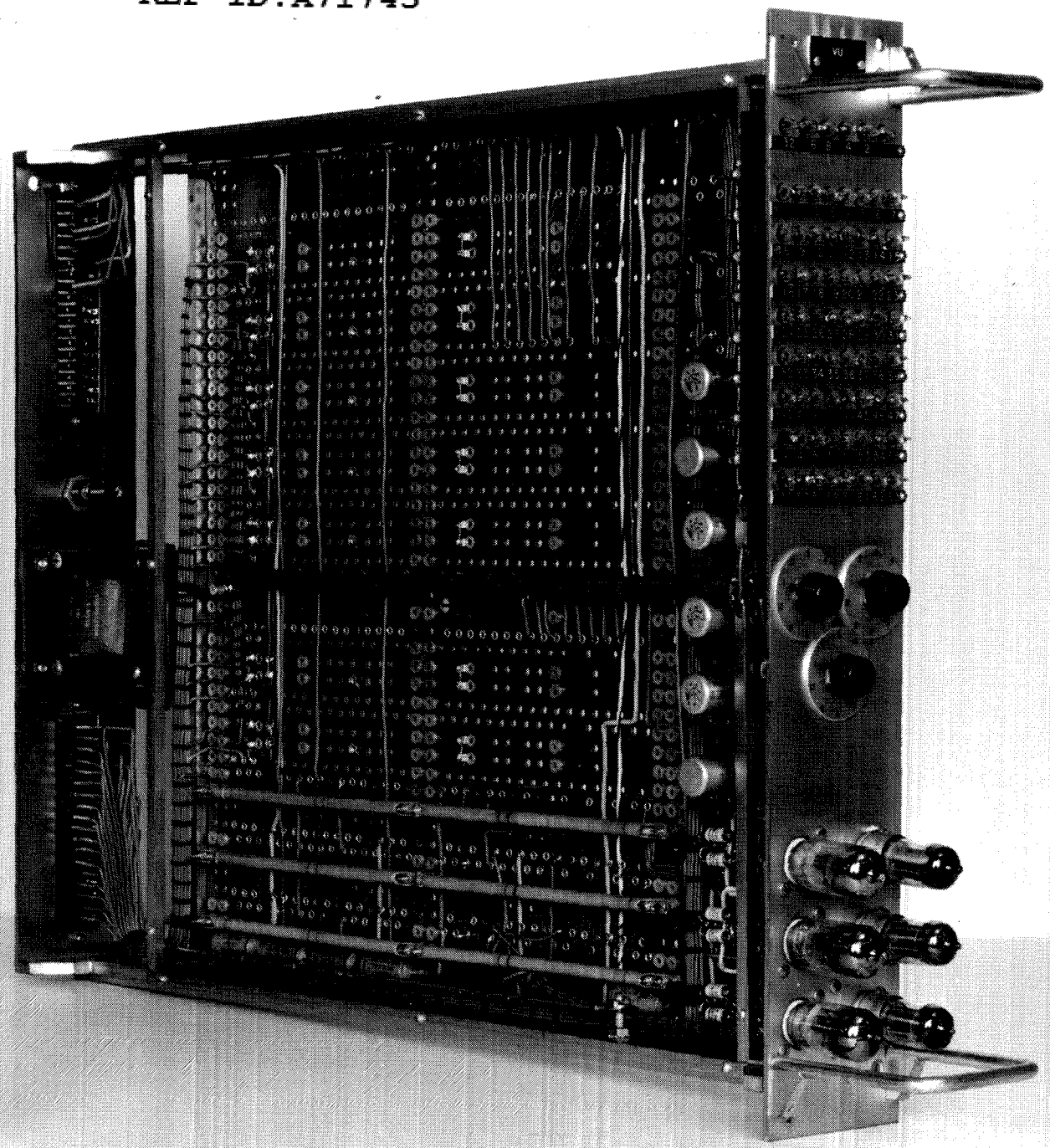


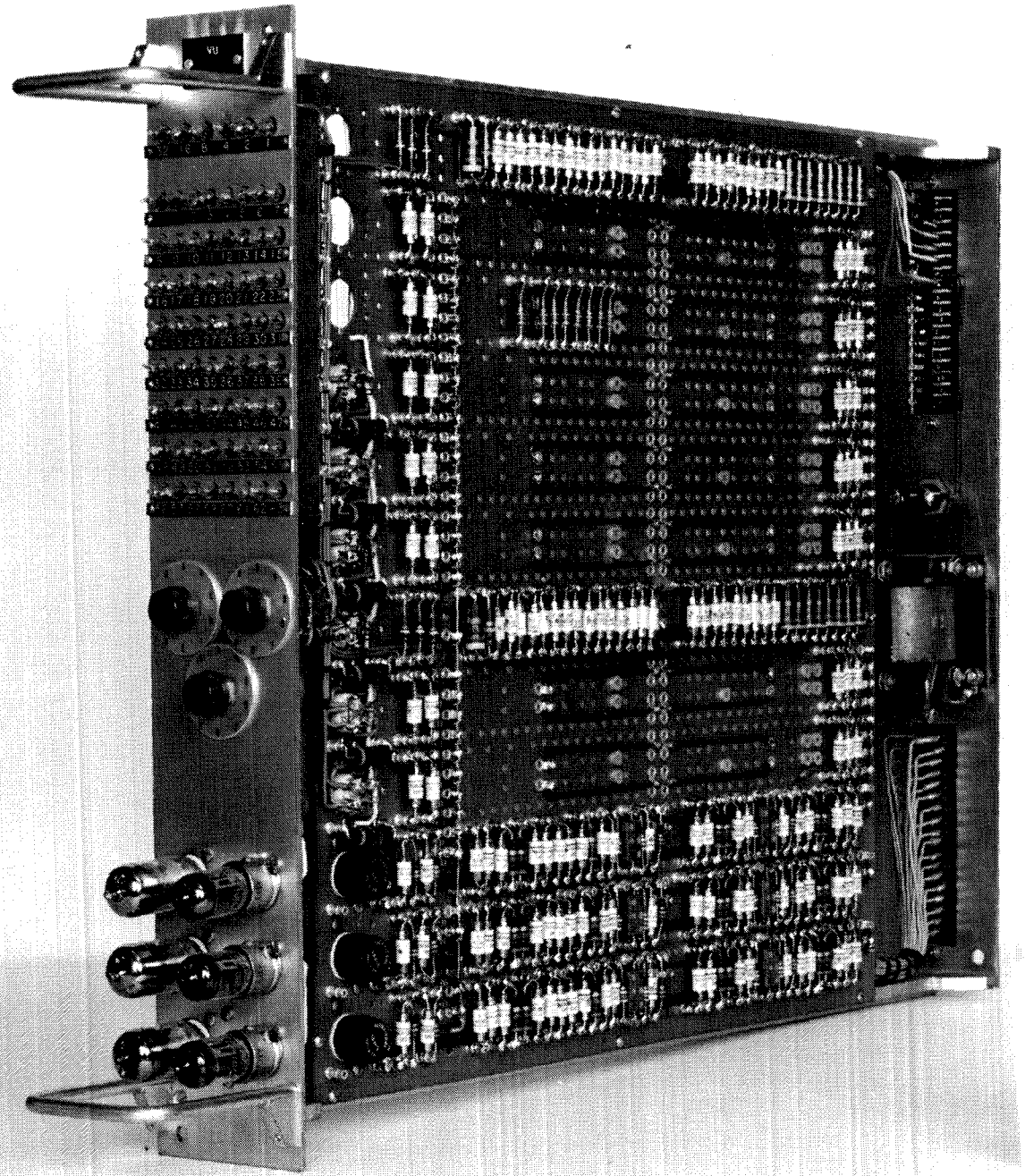
NOTE

SIMILAR SWITCH STRUCTURES ARE ASSOCIATED WITH TUBES 2 & 3

VISUAL UNIT



V.U.



V.U.

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CHAPTER 4

THE MOD-COUNTER (MC)

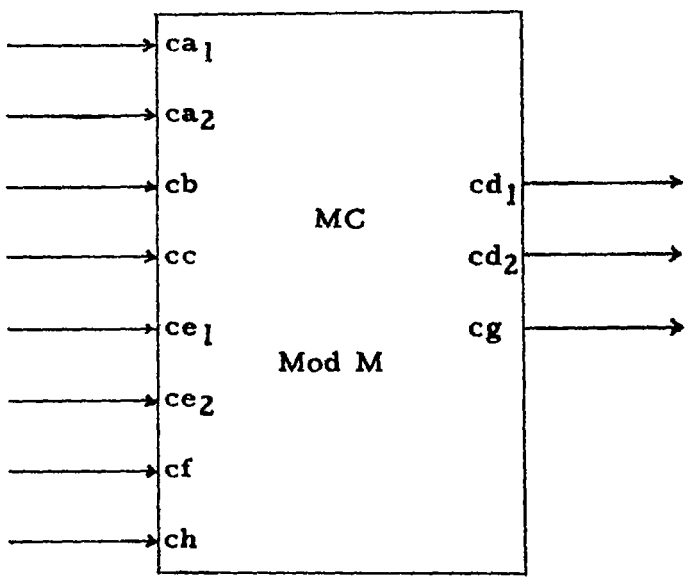
I. Function

Counting is a very common operation in the functioning of analytical machines, but frequently counters are designed around a fixed modulus such as 10 or some power of 2. In DERVISH, however, the object was to design a counter with a settable modulus and enough flexibilities for a number of applications.

The Mod-Counter now designed to count at a maximum rate of 167,000 counts per second operates on a six microsecond time cycle. It is suitable for a variety of applications and may be adjusted for any modulus up to and including 64. It is also capable of counting at a rate of either +1 or +2.

II. Symbolic Representation

The following sketch shows how the Mod-Counter may be represented in a block diagram:



Leads ca_2 and cb have facility for one microsecond plug-in delay lines to permit counting at a +2 rate. Also, leads ca_2, cc, ce, and cf have plug-in delay lines up to 1.00 microsecond to permit the use of signals which may occur early by that amount with respect to the prescribed time. These delays are ignored in the following discussion except where specifically noted.

The functions of the leads may be defined as follows:

cb - Count Input. This lead must have pulses at all times when no count is being made. For each count a blank must occur at $_3T_6$.

ca_1, ca_2 - Count Control. The signals on these leads determine when counts are made. If neither lead is used, a count is made solely by the blank at $_3T_6$ on lead cb. If ca_1 is used, a count is made when both cb and ca_1 have a blank at $_3T_6$. If both control leads are used, a count is made only when blanks occur at $_3T_6$ on leads cb, ca_1 and ca_2 simultaneously.

cc - Reset. This lead must have pulses at all times normally. Reset takes place when a blank occurs at $_3T_6$. The blank may be followed by 1 to 5 additional blanks during the reset cycle without harm.

ch - Reset Control. The signal of this lead controls the reset action of the signal on lead cc. When this lead is not used, a reset is effected for each occurrence of a blank at $_3T_6$ on lead cc. When this lead is used a reset is effected only when blanks occur on both ch and cc at $_3T_6$.

cf - Mod Input. This lead must have a pattern of negative going pulses timed P_1 at $_2T_1$ for the value of the modulus minus one.

ce_1, ce_2 - Preset Count. For normal reset to zero, one of these two leads requires a constant stream of pulses during the reset cycle. For a reset to some other value such as 5, the lead that is used must have a pattern of pulses for the value 5 timed P_1 at $_4T_6$ during the reset cycle. Both leads can be used in the case where the Mod-Counter is preset to some value within its operating range then resets to zero each time thereafter. For example, ce_1 could be supplied with a continuous stream of pulses (representing zero) and ce_2 supplied with a preset pattern representing some other value. The cyclic reset would always be to zero since the pattern on ce_1 would over-ride that one ce_2 but when an initial reset is made, the pulses on ce_1 could be stopped, thereby allowing a preset to the value of the pattern on ce_2.

cd_1 - Output. This output is timed P_1 at $_4T_6$ and could be considered as the value of the count just prior to the next count.

cd_2 - Output. This output it timed P_1 at $_1T_1$ and is always the newly formed count whether reset or just after the most recent count is added.

cg - Carry Indicator. This lead is not a true carry indicator but rather it indicates that the content of the counter has built up to its highest value

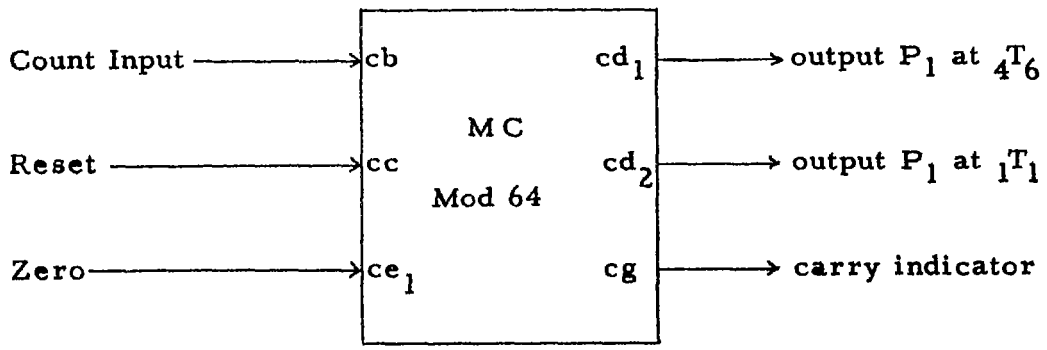
as evidenced by a comparison match with the mod input on lead of. This means that when the next count is added the contents of the counter must return to zero on a preset value. This is the same as indicating when the counter has reached the end of a cycle.

It is not necessary to use all input leads at all times, especially those put in for control purposes. For example: the count control leads ca_1 and ca_2 are not required for counting but are provided so as to make the process of counting subject to conditions. The application will determine how many of these leads are to be utilized.

III. Applications and programming considerations

A. Simple Counting

For simple straight counting, a minimum set of connections to the counter need to be used. The following sketch shows this representation:



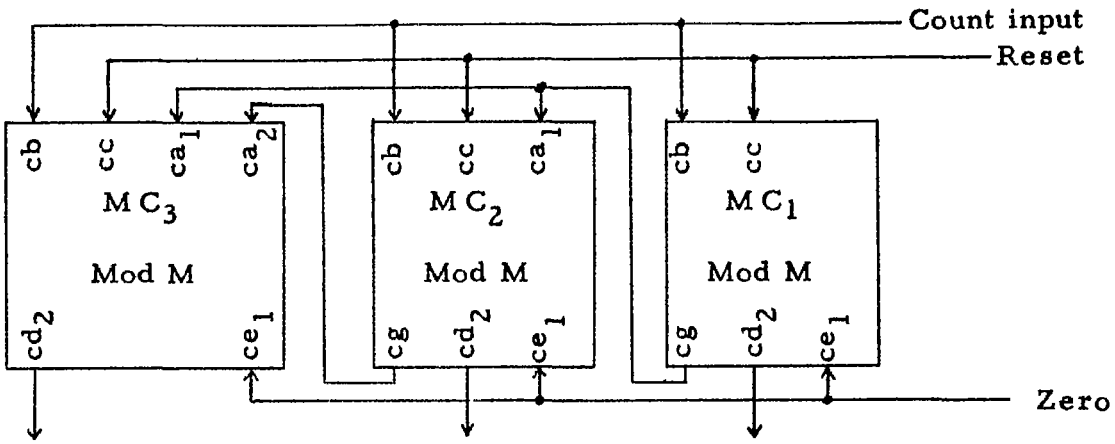
Totals not in excess of 63 will accumulate in the counter and be available for output on lead cd_2 with P_1 at $_1T_1$ or 5 3/4 microseconds later on lead cd_1 with P_1 at $_4T_6$. The indication that the count has reached 63 is provided by the occurrence of a blank on lead cg at $_3T_6$.

B. Cascade Counting

(1) For Moduli up to 64:

When it is desired to count items whose total exceeds 63, two or more Mod-Counters may be operated in series or cascade. When this is done, the connections to each counter are similar to those used when a counter is used by itself. The main difference occurs in the control of the successive units.

The following example shows three counters in cascade:



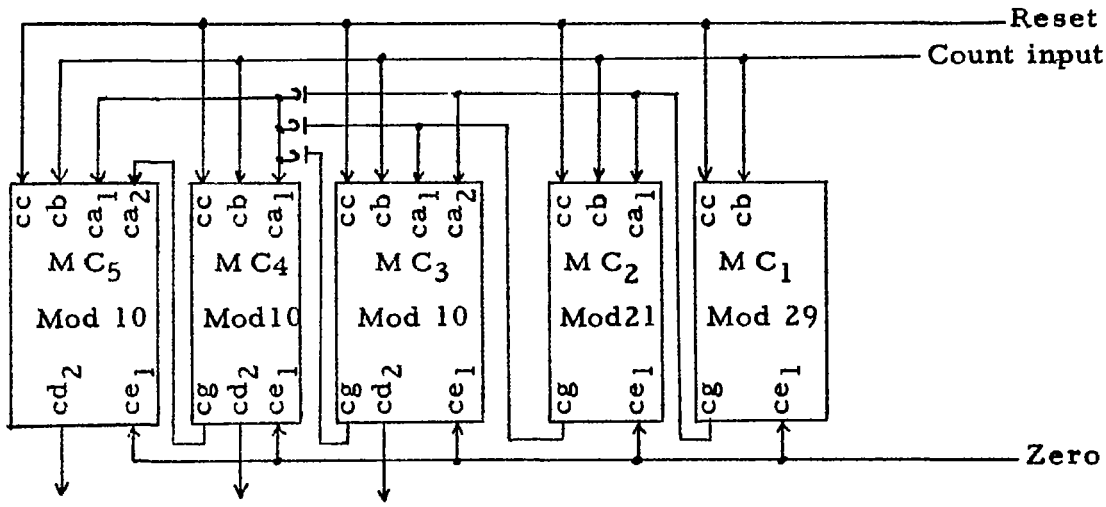
This is a good example of a straightforward metric arrangement regardless of the modulus. By using a modulus of 10, however, a normal decade is represented.

(2) For moduli greater than 64.

(a) Factorable moduli.

In the above example of counters used in cascade, the same modulus may be used for each counter to produce a regular counting sequence but a different modulus may be just as easily applied to each counter to produce a somewhat irregular counting sequence. In either case, the evaluation of the total count in the cascade is the sum of the products of the contents of each counter times the modulus applied to its controling predecessor.

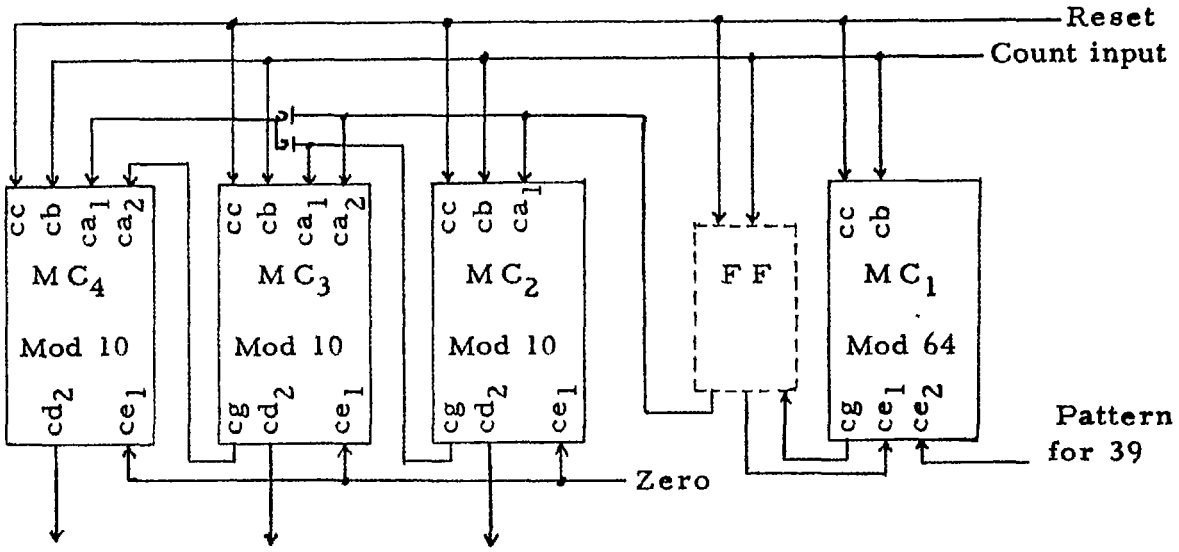
The following example shows how the product of two different moduli can be used to effect or simulate a large modulus:



In this normal cascade arrangement MC_1 counts every item, MC_2 counts every 29th item, and MC_3 counts every 209th item. This is an easy means of obtaining a large modulus provided none of its factors are greater than 64.

(b) Non-factorable moduli

It is also possible to obtain a non-factorable modulus between 64 and 128 such as 89 using an external flip-flop in conjunction with a Mod-Counter. The following sketch shows this:



The flip-flop has two functions: (1) to control the counting of MC_2 in such a manner that MC_1 counts up to its upper limit twice for each count entered into MC_2; (2) to control the ce_1 input to MC_1 in such a manner that MC_1 alternates between two counting ranges 0 - 63 and 39 - 63.

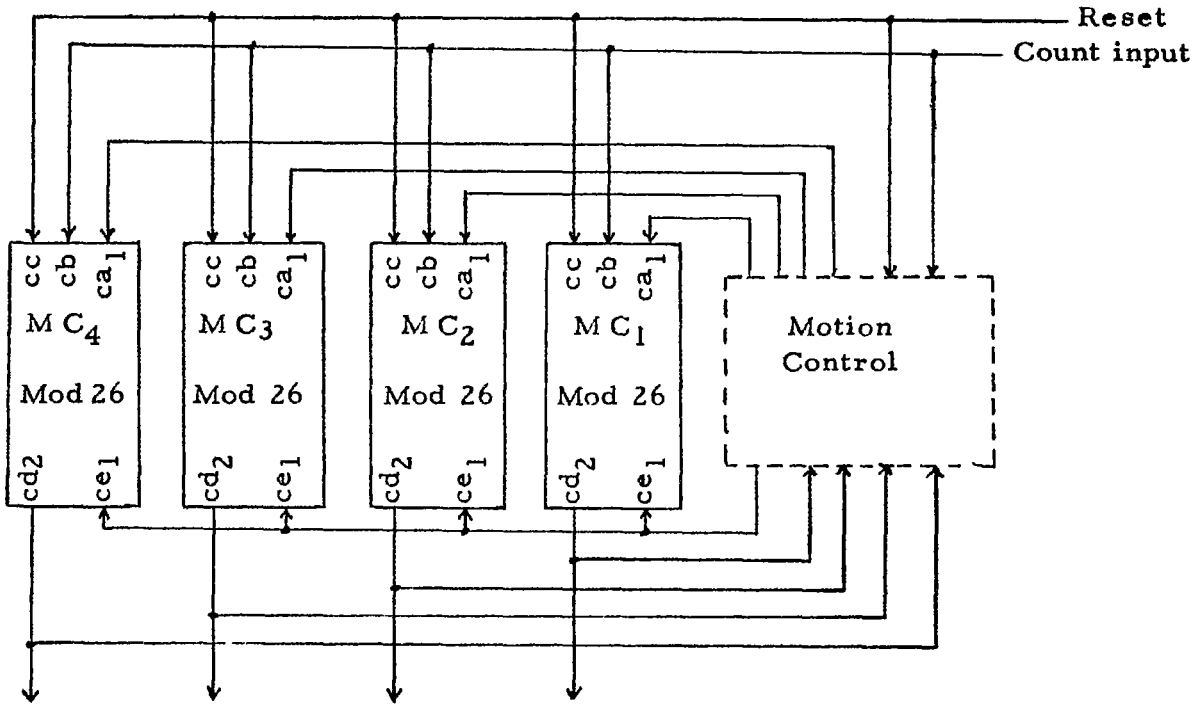
The sum of the lengths of the two ranges would, therefore, represent a modulus of 89 (64 + 25) or a rate at which MC_2 would be allowed to count. The two ranges might just as well be 0 - 44 and 1 - 44 giving lengths of 45 and 44 or any other two lengths whose sum is 89 provided they both have the same top value and not greater than 63.

C. Rotor Position Indicator

The process of indicating consecutive positions of a cipher machine rotor is really nothing more than counting the successive times it has been stepped from some starting point. The Mod-Counter is ideally suited

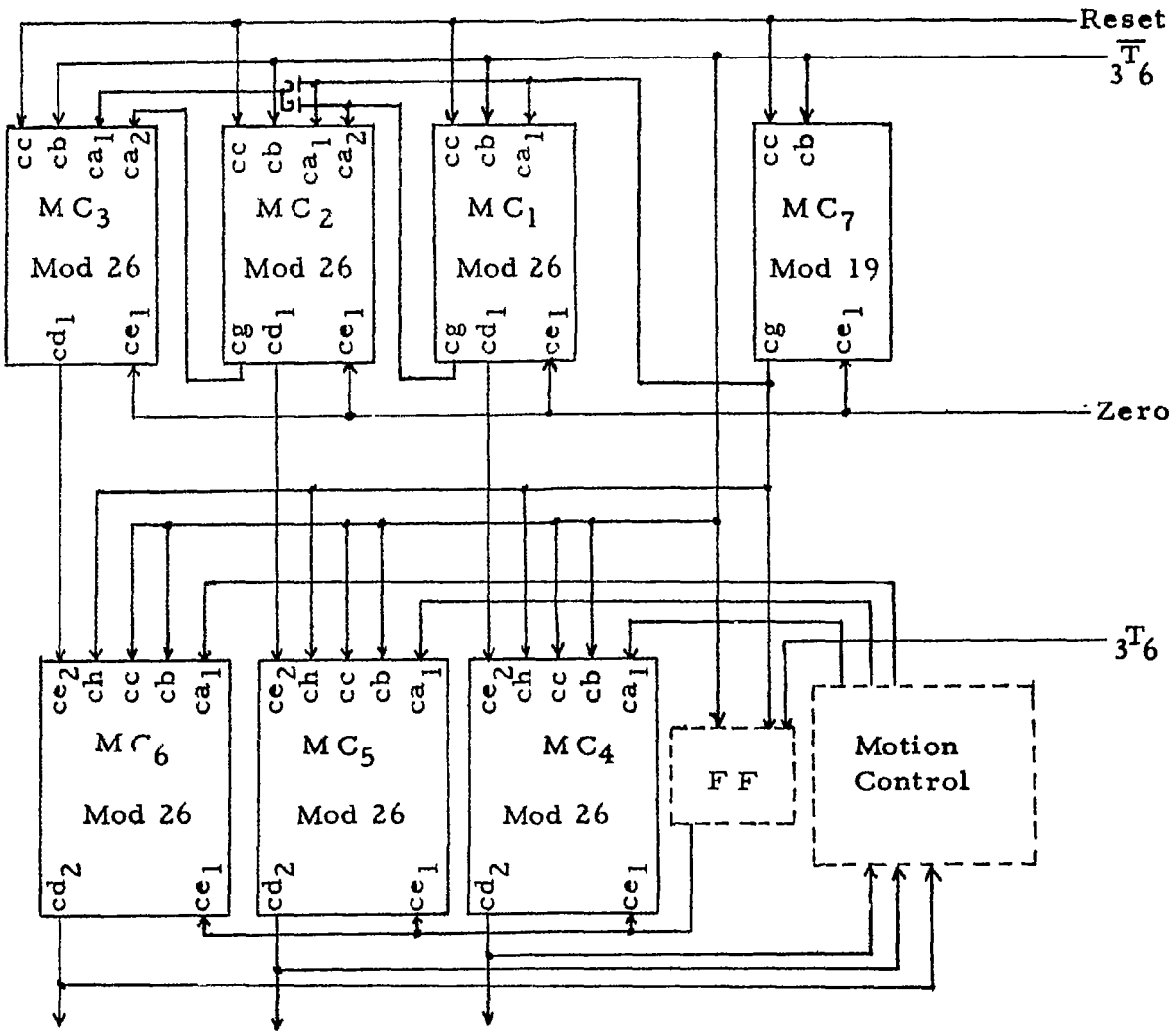
for this purpose. A 26-point rotor has positions that can be represented by 0, 1, 2, 3, ... 25, 0, 1, ... etc. This represents successive counts on a modulus of 26. The stepping of the rotor can be controlled since the counting is subject to conditions on leads ca_1 and ca_2. It can be seen that a rotor ensemble may be represented by a group of mod-counters whose stepping may be controlled according to some motion pattern applied to their various ca leads. They can be reset to any position from which to start a stepping sequence since the Mod-Counter can be reset to zero if lead ce_1 contains a continuous stream of pulses or to some other value represented by the pulse pattern on lead ce_2 if lead ce_1 has no pulses. The pulse pattern source for lead ce_2 may be some fixed pattern, another Mod-Counter controlled to provide consecutive reset values, or some other generator source.

The following sketch shows how rotor positions of a 4 rotor ensemble may be generated:



The Motion Control in the foregoing sketch is shown merely to indicate the connections to the Mod-Counters, especially the ca_1 leads. In the normal sense the positions of a rotor may control the stepping of another so the cd_2 leads are shown going into the Motion Control. The ce_2 leads should be supplied with patterns of pulses representing the positions to which the rotors reset.

Since the Mod-Counter has a basic cycle period of 6 microseconds it is possible to produce 167,000 successive rotor positions per second. The time for resetting to a new position is the same as for stepping. The following sketch shows how seven Mod-Counters can be connected to represent rotor positions in an array of three 26-point rotors which step 19 positions in their motion cycle from every possible starting point or setting:



The foregoing sketch may be considered to consist of three parts: (1) a metric type counter consisting of MC_1, MC_2 and MC_3; (2) the position indicators MC_4, MC_5 and MC_6; and (3) the controling units consisting of MC_7, FF and the Motion Control. The function of the first part is to supply the second part with a new reset value every cycle, and to do this it must count one position each 19 cycles. MC_7 provides an easy method of deriving a 19 character cycle. The function of the second part is to generate the 18 succeeding positions from each starting point of the three

rotors whose stepping is controlled by the Motion Control. The third control element is a flip-flop normally generating a continuous stream of pulses but is turned off for 6 pulse times every 19th cycle allowing MC_4, MC_5 and MC_6 to be reset to the respective values in MC_1, MC_2 and MC_3 which then advance to the next position. This means that after a reset of MC_1, MC_2 and MC_3 successive starting points 000, 001, 002, 003, etc., will each be used as the first position of a 19 step cycle of the rotors.

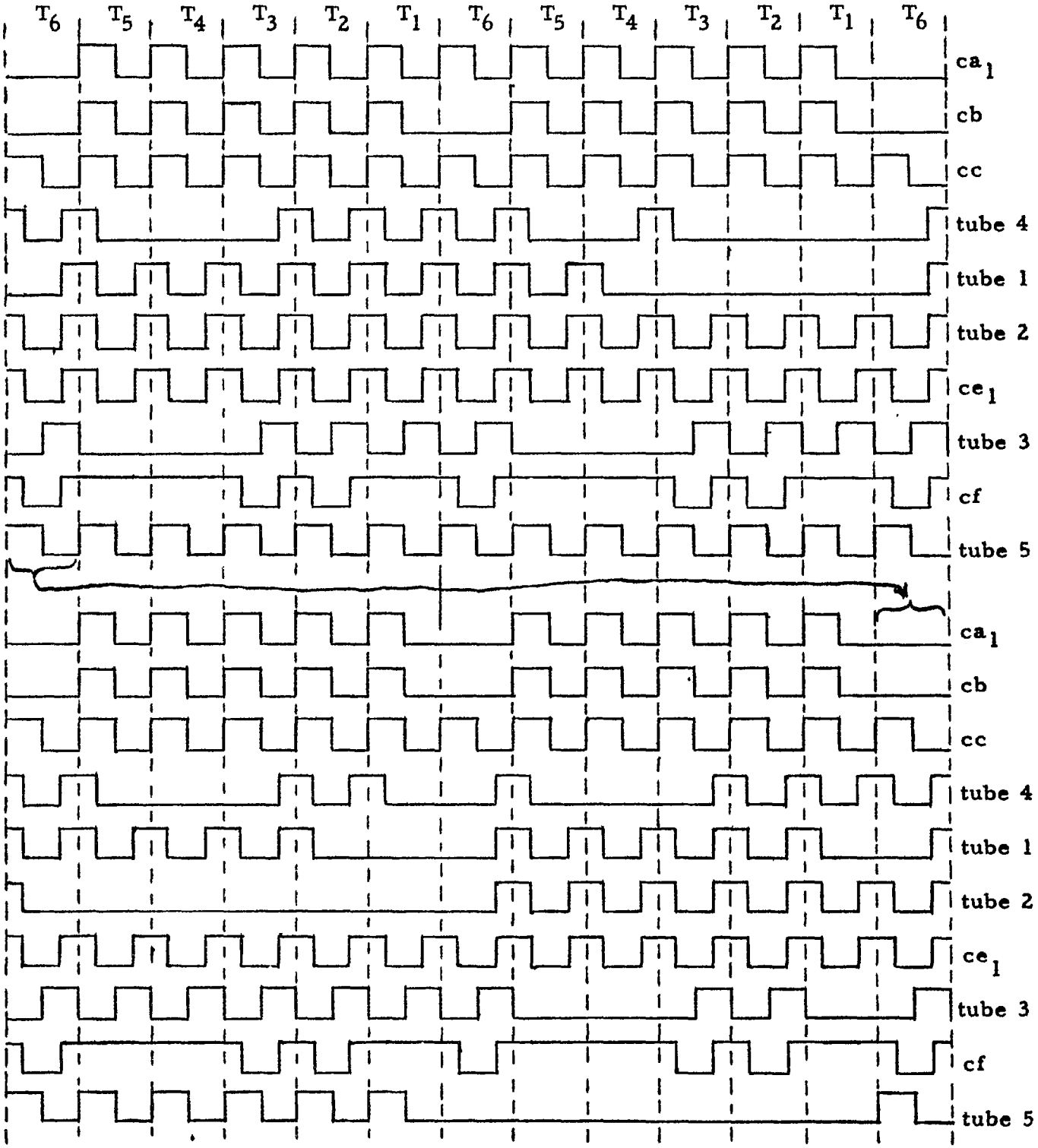
IV. Operation

The heart of the counter consists of an add-one circuit in a 6 microsecond delay line storage loop. Three tubes with associated gates accomplish this function but two more tubes are used in order to provide the functions of reset and carry indication. The timing in this unit is chosen so the output of tube 3 is P_1 at ${}_1T_1$ as shown on the first logical diagram. An alternate timing may be used whereby the output of tube 4 is P_1 at ${}_1T_1$ as shown on the second logical diagram. In the following description the negative signals are omitted.

In normal operation, according to the first logical diagram, tubes 1 and 2 put out continuous pulse trains and the six bits representing the count N circulate in a closed loop consisting of tubes 3, 4 and a 5.50 microsecond delay line. Tube 1 puts out a blank, or no pulse, in the P_1 position when 1 is to be added to the count circulating through tube 4 and puts out one additional blank for easy carry over into a next higher pulse position. Tube 3 forms the sum N + 1. Tube 2, while running continuously, enables the count to be held in the loop but turns off for six microseconds when the counter is reset. The reset can be effected either by a blank signal on lead cc and lead ch or when tube 5 is off and 1 is added to N. The comparison tube 5 is off at ${}_3T_6$ only when the circulating count has grown until it has become equal to one less than the mod capacity of the counter. This indicates that on the next count added, N should return to zero or some other preset bottom value as determined by the signals on leads ce_1 and ce_2. It is not necessary to use both these leads at the same time and in cases where only one is needed either one may be chosen since they both drive the same "OR" gate. How they can be used to select zero or some other number for presetting is more fully demonstrated in Par. III C.

A provisional count control is made possible by leads ca_1 and ca_2 and provisional reset by lead ch. Their patterns of pulses are not critical except at ${}_3T_6$ when they must be correct. At all other times they have no effect on the circuit. An example of the use of one of these leads may be shown when two or more counters are cascaded as covered in Par. III B.

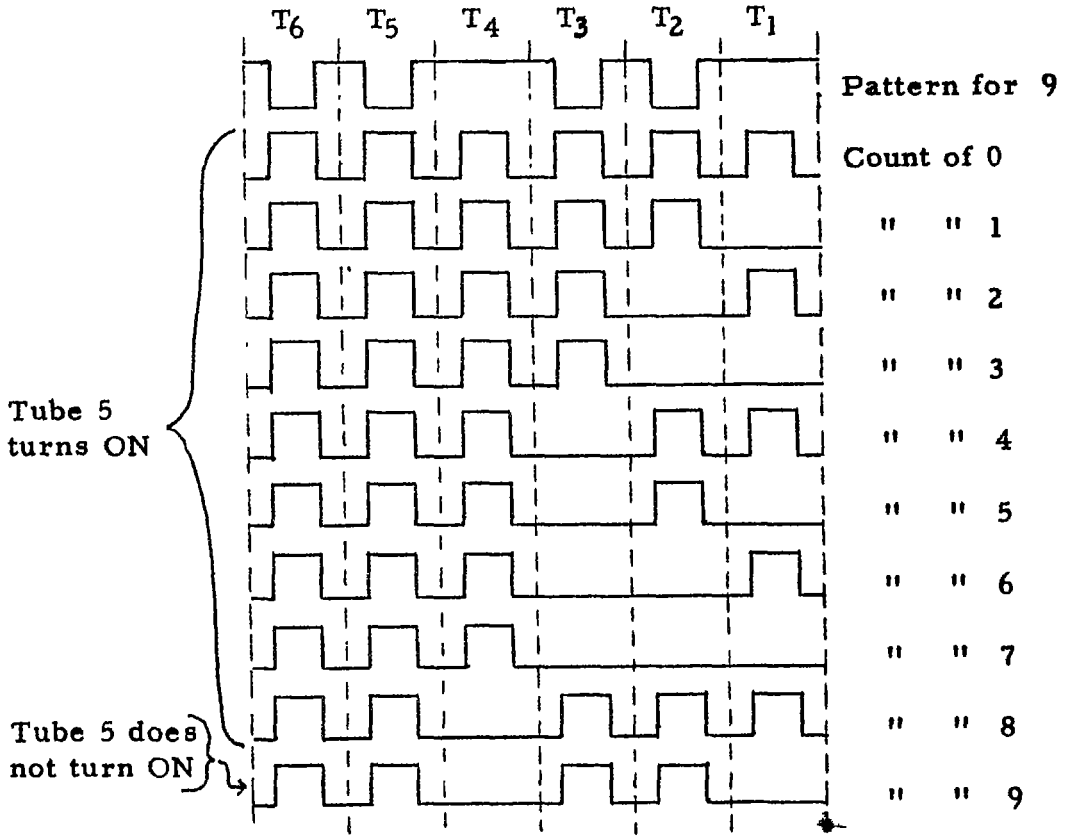
The following sketch shows pulse patterns at various points in the counter through four cycles with a modulus of 26 and a circulating count of 23:



It can be seen in the foregoing example that on the fourth cycle the output of tube 3 could have been a pattern of pulses from lead ce_2 provided the stream on ce_1 had been made blank for those six microseconds. Since ce_1 had a continuous pattern during that cycle no existing pattern on ce_2 could have had any effect on tube 3. By controlling the pattern on ce_1 to be OFF or ON at the proper time, the counter can be preset to some value, within its counting range, other than zero.

In order to demonstrate how the "AND" gate of tube 5 detects when the count in the counter has built up to its top value, assume a modulus of 10 which means lead cf should contain a pattern of negative going pulses timed P_1 at $_2T_1$ which represents (10-1) or 9. The pattern for the value 9 will fail to inhibit the "AND" gate action during at least one pulse position for all counts 0 through 8 causing the flip-flop of tube 5 to turn ON. When the count of 9 is reached the inhibition pulses on lead cf coincide with all the enabling pulses in the count pattern and the flip-flop of tube 5 does not turn ON, so the signal on lead cg is blank at $_3T_6$ indicating that the full count is reached. The next occurrence of a count will cause tube 2 to turn OFF for 6 microseconds thereby enabling tube 3 to put out the reset value.

Pulse patterns on the "AND" gate of tube 5:



V. Physical Characteristics

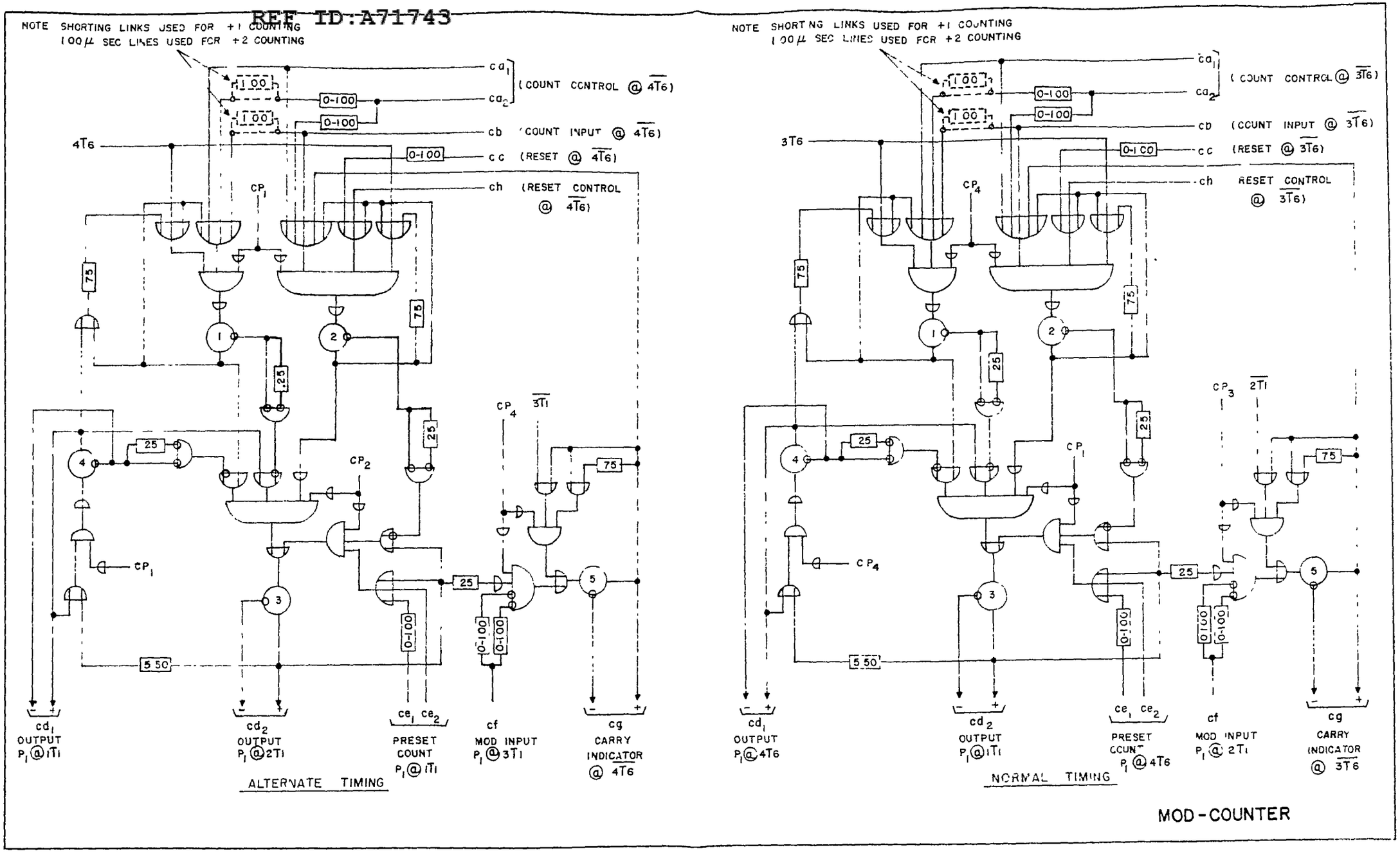
Four complete and separate Mod-Counters are built on one chassis with all input and output leads available on the two plugs at the back of the chassis. The four units are functionally independent but are tied together electrically. The circuit component requirement for one chassis of four Mod-Counters is approximately as follows:

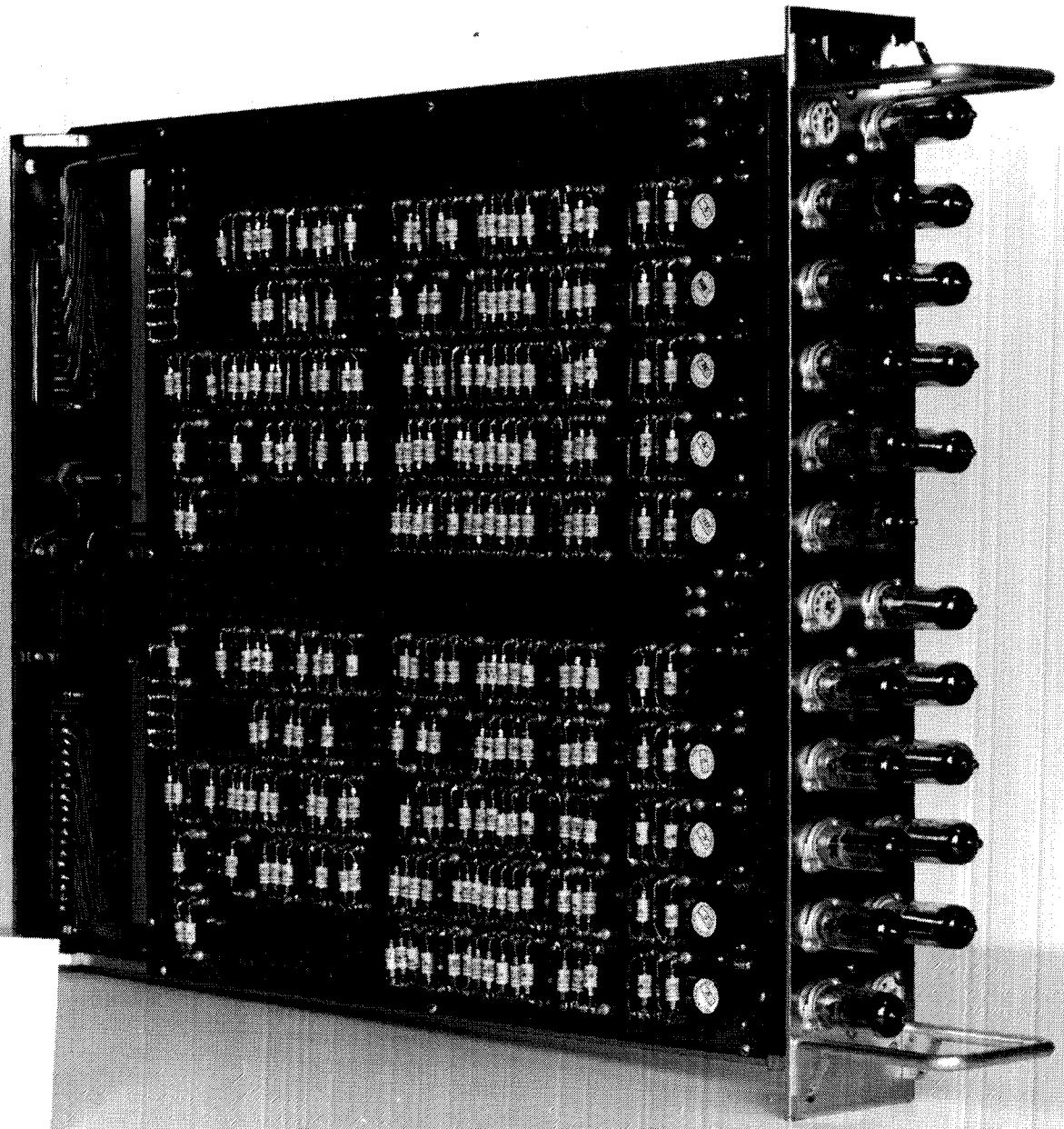
Vacuum tubes:	20 type 6AN5
Pulse transformers:	20 plug-in ferrite type
Crystal diodes:	425 type 1N34, CK705, or comparable type
Delay lines:	52 sticks of one microsecond or fraction
Resistors:	232
Filament transformers:	1 Thordarson type T21F12

The power requirement for one chassis varies somewhat due to resistor values used but an average approximation for the power consumption on the more important voltages is as follows:

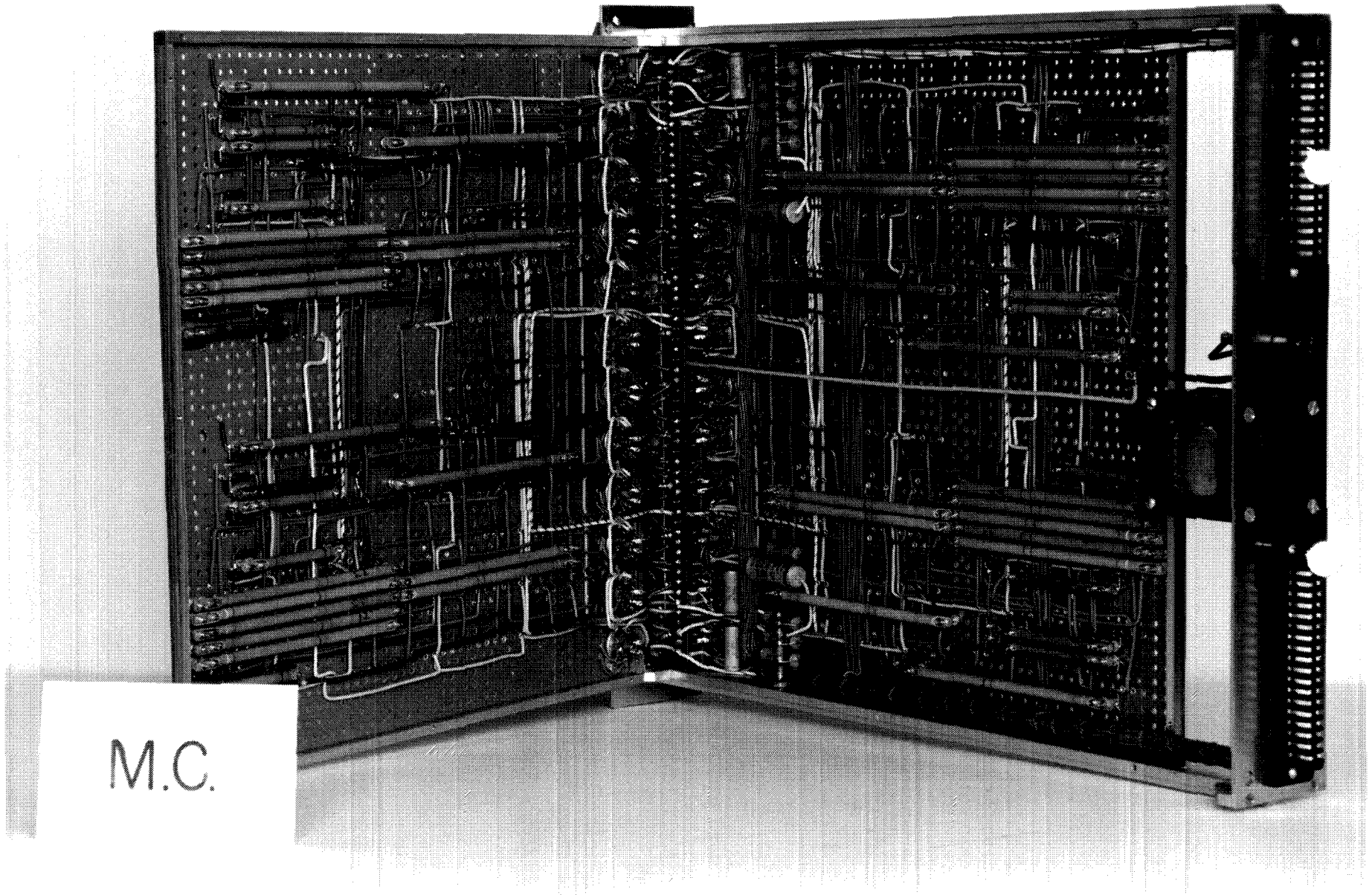
	Current	Watts
+200V	0.4 amp.	80
+62V	0.5 amp.	31
-8V	-0.25 amp.	-1
-65V	0.9 amp.	58
110V a-c	0.55 amp.	60

The total power dissipation is approximately 230 to 250 watts which represents a heat dissipation of 13 to 14 B.T.U. per minute.



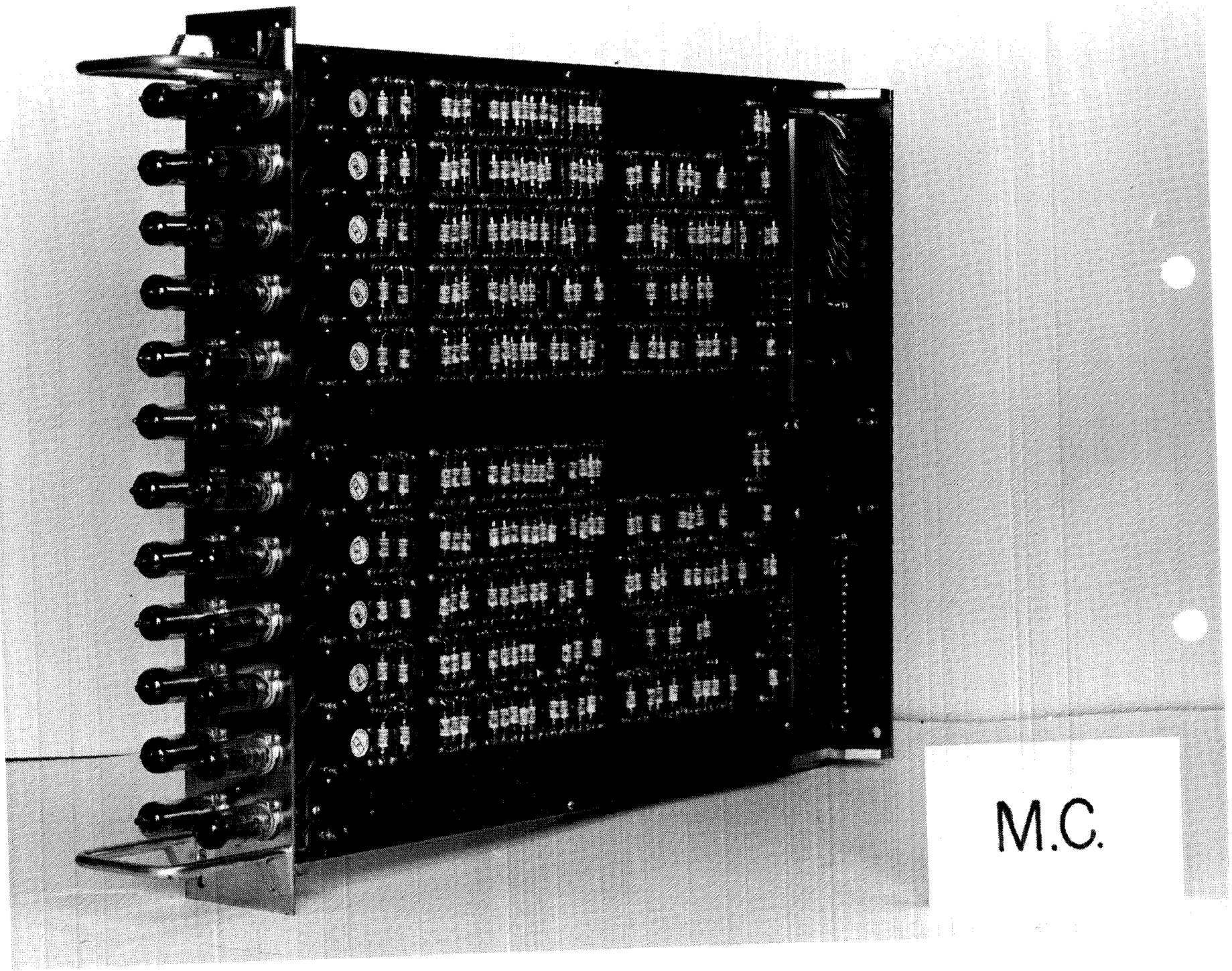


M.C.



M.C.

REF ID:A71743



M.C.

CHAPTER 5

THE MOD-ADDER (MA)

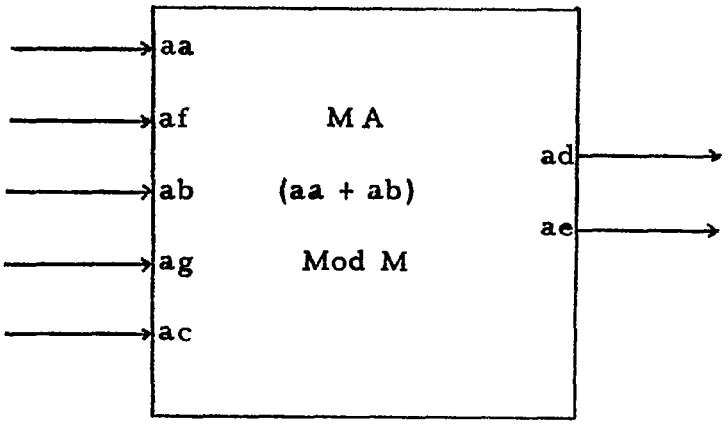
I. Function

The Mod-Adder performs three independent functions with equal ease and facility. Notes 1, 2, and 3 on the logical diagram indicate the arrangement of five plug-in delay line sticks or connecting links to be used to make the unit function as a Mod-Adder, a Mod-Subtractor or an Absolute Differencer. When the function of modular addition is being done, the sum of two numbers is formed and adjusted according to some preset modulus and the result is supplied as an output. When the function of modular subtraction is being performed, the difference of two numbers is formed and adjusted according to a preset modulus and the result supplied as an output. When the function of forming an absolute difference is performed, the smaller of two quantities is subtracted from the larger and this difference provided as an output.

In all three modes of operation, the same general characteristics apply, in that one 6 microsecond cyle is consumed in each operation, each data input consists of a 6-bit quantity represented in serial binary form timed with P_1 at ${}_1T_1$, and the output is a 6-bit quantity in serial binary form timed P_1 at ${}_1T_1$. In all cases, no input quantity can be equal to or greater than the modulus, which in turn, must be equal to or less than 64.

II. Symbolic Representation

The following sketch shows how the Mod-Adder may be represented in a block diagram:



The functions of the leads may be defined as follows:

aa, ab - Inputs. These leads are to be used for supplying the two operands to the Mod-Adder. The pulse patterns should be timed P_1 at ${}_1T_1$.

af, ag - Input controls. When these leads are not used, the inputs on leads aa and ab feed in normally. When they are used, they pass or stop the signals on leads aa and ab respectively. For example, when af is used, it must be supplied with pulses all times that the input on aa is to be prohibited from entering the adder and blanks when the input on aa is allowed to enter the adder.

ac - Mod input. This input is for the modulus and must be timed P_1 at ${}_2T_1$.

ad - Output. This lead provides the output result timed P_1 at ${}_1T_1$.

ae - Exceed indicator. This lead indicates when the result of the modular addition or subtraction required adjustment to be correct. For example, during the output cycle, lead ae will have six pulses if the sum of the input quantities is less than the modulus or it will have six blanks if the sum of the input quantities is equal to or greater than the modulus.

III. Application and Program Considerations

A. Nominal Use

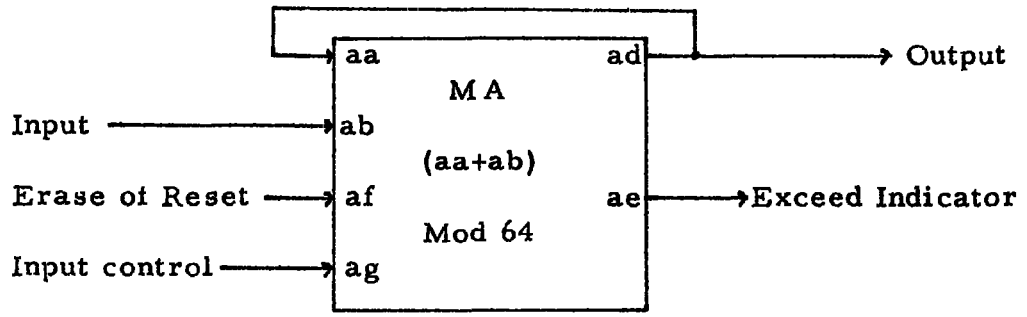
The simplest application of the Mod-Adder is that of just forming a sum, or difference, of two 6-bit quantities and adjusting the result to some modulus. It was first designed to fulfill one specific requirement, namely to represent the relative displacement of two items when the absolute displacement or position of each is known. For example, if item A was moved 12 miles due west from a given starting point and item B was moved 3 miles due west from the same starting point the relative displacement of A with respect to B is (12-3) or 9 miles due west.

B. Accumulation

(1) For totals less than 64.

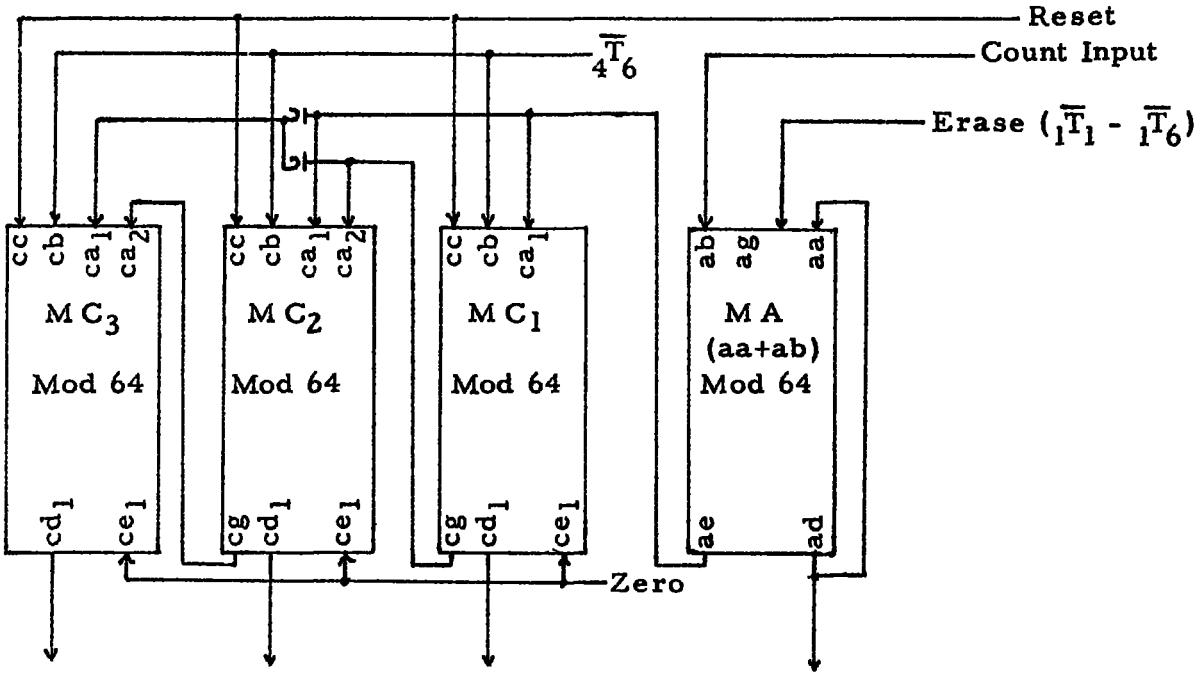
The Mod-Adder is readily adaptable for use as a 6-bit modular accumulator so long as each quantity being accumulated is less than the modulus. By using its output on lead ad as an input on lead aa, the growing sum circulates around on a six microsecond cycle and quantities fed in on lead ab

are added into this sum. Lead af provides an erase or reset to zero feature while lead ag can be used as a suitable control to add zero or some quantity from lead ab. The following sketch shows this arrangement:



(2) For totals equal to or greater than 64.

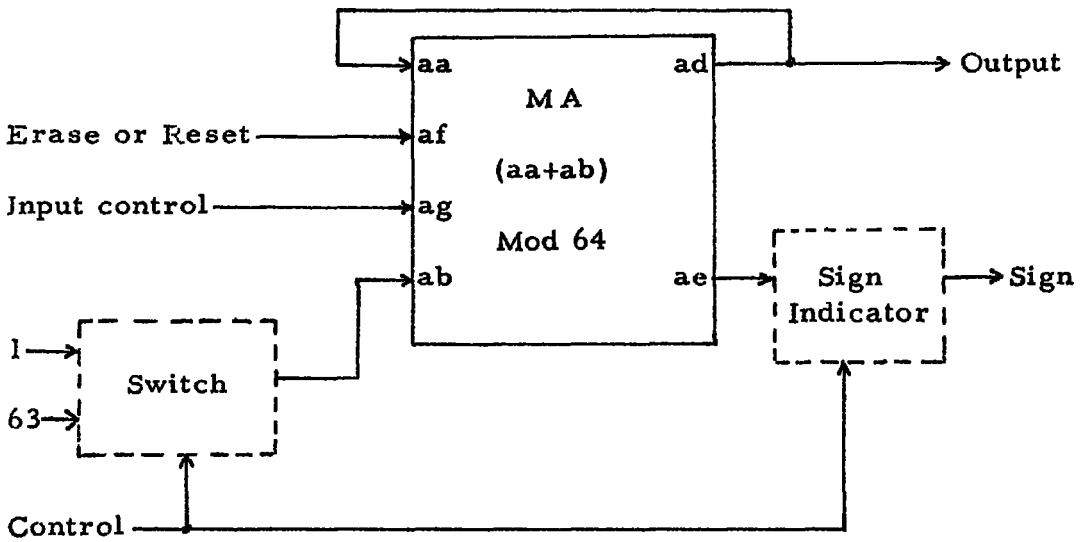
When it is desired to accumulate quantities whose total is 64 or greater, an arrangement consisting of one Mod-Adder and some Mod-Counters can be made to form an accumulator whose capacity is more than 6 binary places. In this use the alternate timing for the Mod-Counter needs to be used. The following sketch shows an example of an accumulator with a 24 binary place capacity:



The counters serve to count the number of times that the Mod-Adder accumulated over its modulus.

C. Bi-Directional Counting

On certain occasions it is desirable to have a counter which will go backward as well as forward and counters have been built with that facility although they are not in great demand. The Mod-Adder is capable of performing that function when an external electronic switch is provided so that a choice of 1 or 63 may be added to give the effect of +1 or -1. The output must be tied back to one of the inputs as in accumulation. The following sketch demonstrates the idea:

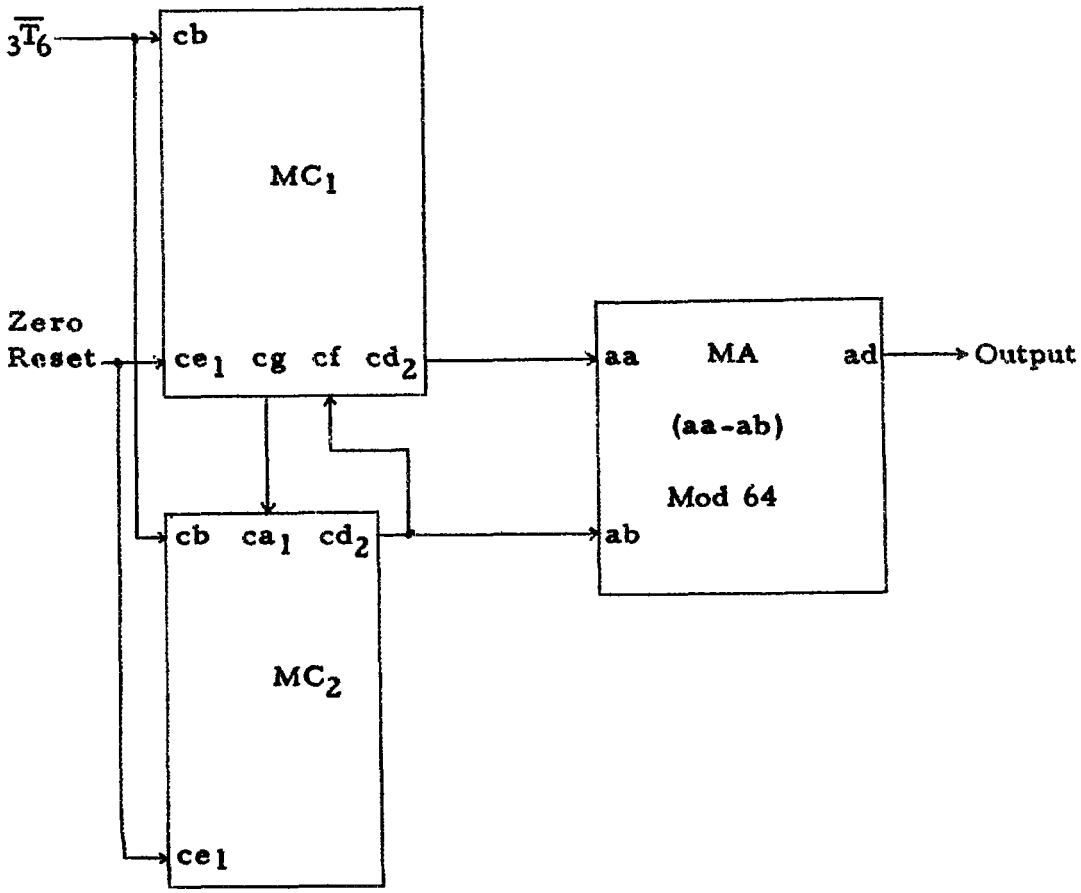


A sign indicator could easily show whether the count in the adder is positive or negative. The circuit condition to control the sign indication would exist when 63 is added into the Mod-Adder and the signal on lead ae shows that the sum (63 - N) < 64. This would only occur when N = 0, or when the counter goes from 0 to -1. When the count is negative, the pulse pattern is not the correct value but 64 minus the correct value. One way of getting around this ambiguity is to have another control on the electronic switch to reverse its selection function when the sign is negative.

D. Generation of Number Sequences

By appropriate arrangements of Mod-Adders and Mod-Counters some rather interesting number sequences can be generated. This is facilitated by the fact that the modulus for a mod-counter may be generated by another Mod-Counter or Mod-Adder. The variety of arrangements is practically

unlimited particularly when they employ units described in next chapters. The following sketch shows a simple arrangement:



In this example MC_1 is the faster stepping counter. MC_2 is stepped each time MC_1 steps past its top value back to zero. Since the output of MC_2 is the modulus input for MC_1 the top value for MC_1 is periodically increased by one. When both MC_1 and MC_2 start at zero the following sequences of numbers are generated:

MC_1 0, 0,1, 0, 1,2, 0, 1, 2,3, 0, 1, 2, 3,4, 0, 1, 2, 3, 4,5,
MC_2 0, 1, 1, 2, 2,2, 3, 3, 3,3, 4, 4, 4, 4,4, 5, 5, 5, 5, 5,5,
MA 0,63,0,62,63,0,61,62,63,0,60,61,62,63,0,59,60,61,62,63,0,

E. Other

There are undoubtedly other uses for the Mod-Adder which may be evident to the reader or which may arise as problem applications are exploited. The examples that have been given are merely suggestive and not limiting.

IV. Operation

In normal operation of the Mod-Adder three input pulse patterns are utilized and two outputs are produced. All pulse patterns are used in both polarities (+) and (-), so hereafter references to pairs of leads will be made in the singular. Two of the input patterns timed P_1 at ${}_1T_1$ are the operands fed in on leads aa and ab and the third pulse pattern timed P_1 at ${}_2T_1$ is the correcting modulus fed in on lead ac. The result or output pulse pattern, timed P_1 at ${}_1T_1$, one character cycle later than the inputs, is available on lead ad. Leads af and ag are provided to permit control of the input quantities on leads aa and ab, respectively. An auxiliary output is available on lead ae which indicates that the modulus correction had to be made for addition or subtraction or that a 2's complement had to be formed in the case of minor differencing. A 2's complement of N when 6-bit quantities are used is equal to $(2^6 - N)$.

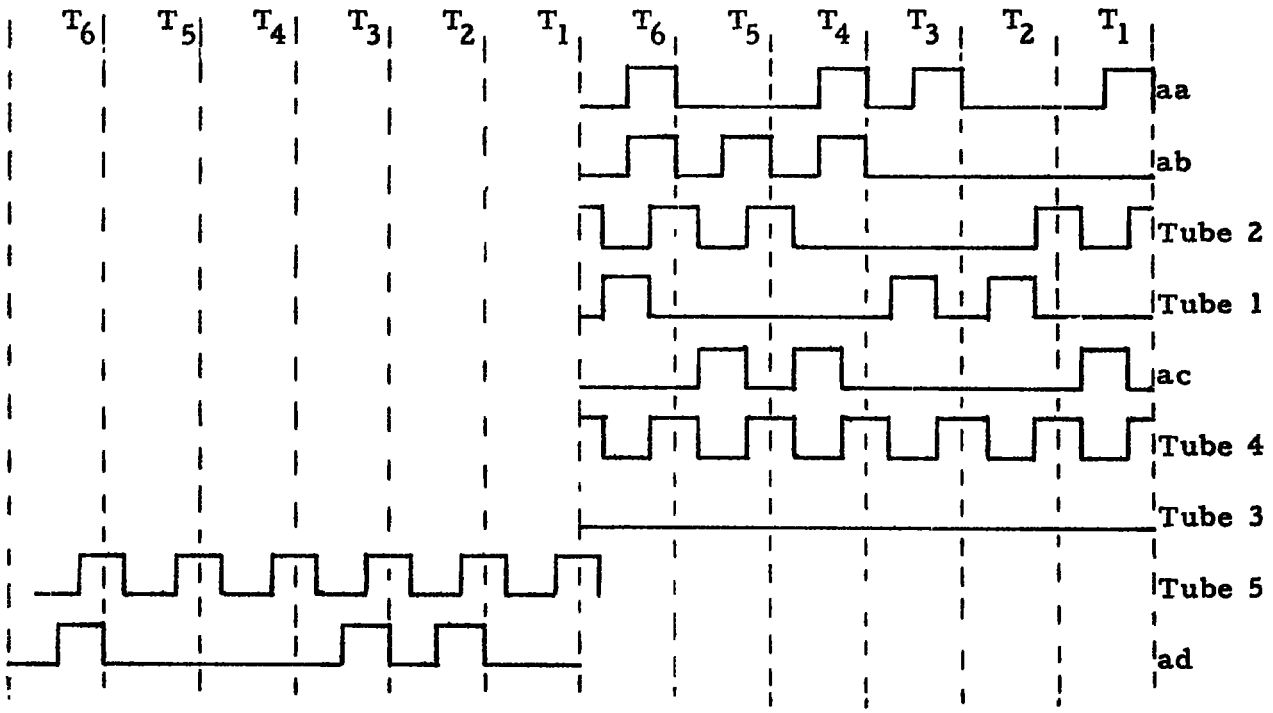
There are three distinct sections of the circuit which are: (1) the first section made up of tube 1, an adder-subtractor tube, and tube 2, a carry-borrow tube; (2) the second section made up of tube 3, an adder-complementer tube, and tube 4, a carry tube; and (3) the output section composed of tubes 5 and 6. In the first section, a sum or difference is formed from the signals on leads aa and ab. This result is added in the second adder to a pulse pattern on lead ac to form a second result. One of these two results is correct, the other incorrect and tube 5 selects the correct one for tube 6 to send out as an output. The condition of carry at the 6th bit position determines which result is correct. The three functions will now be considered in turn assuming a quantity P fed in on lead aa and a quantity Q fed in on lead ab, and a correcting modulus fed in on lead ac.

A. Modular Addition (P + Q) Mod M

The Mod-Adder performs this function when the appropriate arrangement of plug-in delay line sticks or links referred to by Notes 1, 2 and 3 on the logical diagram. When tube 2 is on, the addition rule for tube 1 is: 0 + 0 = 1, 1 + 1 = 1, 0 + 1 = 0, and 1 + 0 = 0. When tube 2 is off, the rule is: 0 + 0 = 0, 1 + 1 = 0, 0 + 1 = 1, and 1 + 0 = 1. The same rules apply to tubes 3 and 4. The two quantities to be added, P and Q, can be any quantities smaller than modulus chosen, but the pulse pattern representing the modulus fed in on lead ac must not be the modulus but rather 64 minus the modulus. For example, to represent a modulus of 10, this pulse pattern should be for the quantity (64 - 10) or 54. The first section of the circuit forms the sum (P + Q) Mod 64 and the second section forms the sum $[(P + Q) \text{ Mod } 64 + (64 - M)] \text{ Mod } 64$. These sums represent (P + Q) and (P + Q - M), respectively. Three distinct cases need to be considered.

Case 1: $(P + Q) < M$

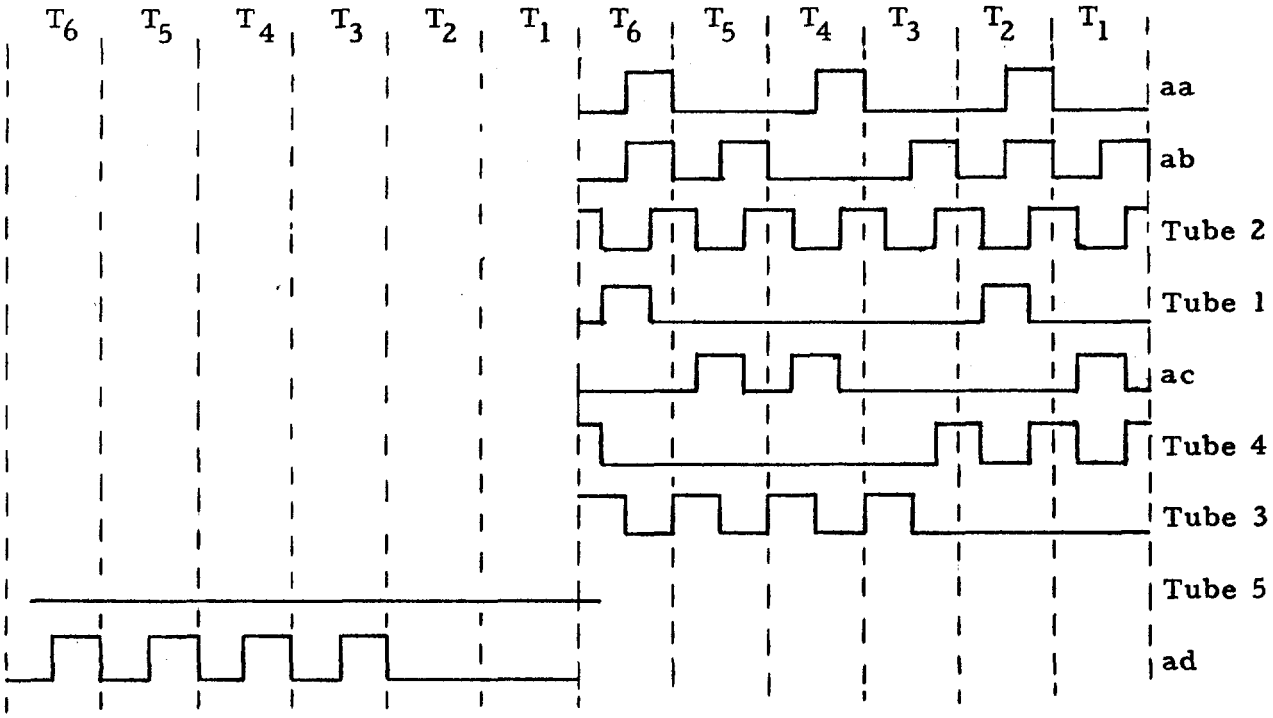
In this case the sum is formed by the first section of the circuit which now functions as an adder, and since M cannot be greater than 64, the sum P + Q cannot exceed 63. Therefore, no carry will be propagated beyond the 6th bit position in the first adder. At the same time, the sum $[(P + Q) + (64 - M)]$ Mod 64 formed in the second section, or adder, of the circuit is also never greater than 63, so no carry will be propagated beyond the 6th bit position, tube 5 will be enabled at the ${}_3T_6$ sampling time and turned on for the next six microseconds thereby selecting the result from the first adder for tube 6 to provide as an output. For example, let P = 18, Q = 7 and (64 - M = 38) where M = 26. The first sum 18 + 7 = 25 which is less than 26 and 25 + 38 = 63 which is less than 64. The following sketch shows pulse patterns at the main points in the circuit for P = 18, Q = 7 and M = 26.



Case 2: $M \leq (P = Q) < 64$

In this case, the sum formed by the first adder is equal to or greater than the modulus, therefore, the corrected sum formed by the second adder is the proper result and the indication of this is the fact that a carry is propagated beyond the 6th bit position in the second adder. Tube 5 is caused to be in the off condition for 6 microseconds because one of its enabling gates has no pulse at the ${}_3T_6$ sampling time, therefore, it selects the sum formed by the second adder for tube 6 to provide as the output. The first adder can

not produce a carry past the 6th bit position since (P + Q) cannot exceed 63 but the second adder does because $[(P + Q) + (64 - M)] \geq 64$. For example, let P = 21, Q = 8 and (64 - M = 38) where M = 26. The first sum (21 + 8) = 29 which is greater than 26 and the second sum 29 + 38 = 67 which is greater than 64. The result is (67 - 64) = 3. The following sketch shows pulse patterns at the main points in the circuit for P = 21, Q = 8 and M = 26:



Case 3: $M \leq (P + Q) \geq 64$

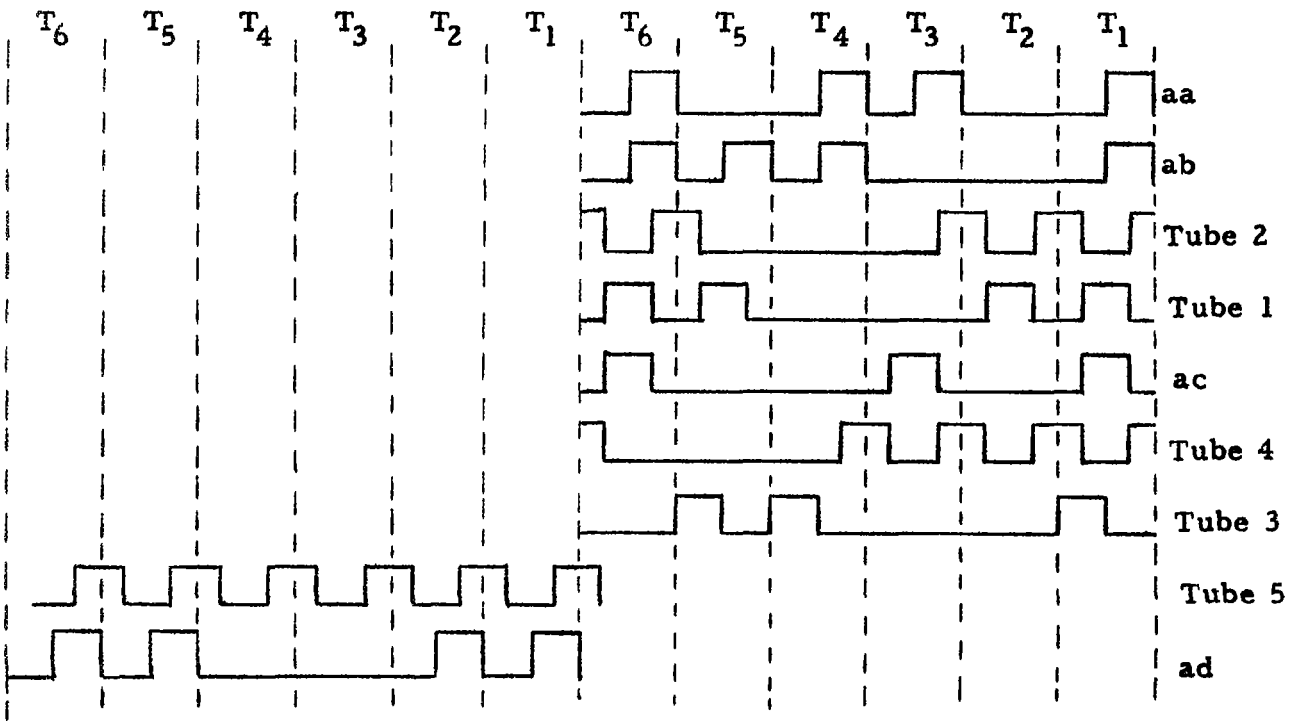
In this case the correct sum is formed by the second adder and the indication of this is the fact that a carry digit is propagated beyond the 6th bit position in the first adder. Therefore, tube 5 is caused to be in the off condition for 6 microseconds just as it was in Case 2, thereby selecting the result formed in the second adder for tube 6 to provide as the output. The second adder cannot produce a carry past the 6th bit position because the maximum possible value for the sum formed in the first adder is $64 - 2\,[64 - (M - 1)]$ which is then added to (64 - M), so the maximum possible value formed by the second adder is $64 - 2\,[64 - (M - 1)] + (64 - M)$ and $2\,[64 - (M - 1)] > (64 - M)$. Therefore, the maximum possible value of the sum formed in the second adder is M - 2. For example, let P = 39, Q = 39 and (64 - M = 24) where M = 40. (39 + 39) = (78 - 64) = 14 and 14 + (64 - 40) = 38 which is equal to (40 - 2). The chief difference between Case 2 and Case 3 is the source of the indication which controls the output selection since in both cases, the output of the second adder is the correct result.

B. Modular Subtraction (P - Q) Mod M

When the function of modular subtraction is to be performed, the appropriate arrangement of the plug-in delay line sticks or links referred to by Notes 1, 2 and 3 on the logical diagram must be made. The first section of the circuit, involving tubes 1 and 2, now functions as a Mod 64 subtractor and the second section as a Mod 64 adder. When tube 2 is ON, the subtraction rule for tube 1 is: 0 - 0 = 1, 1 - 1 = 1, 0 - 1 = 0 and 1 - 0 = 0. When tube 2 is OFF, the rule is: 0 - 0 = 0, 1 - 1 = 0, 0 - 1 = 1 and 1 - 0 = 1. The correct modulus is used and not 64 minus the modulus. The subtractor forms (P - Q) Mod 64 and the adder forms [(P - Q) Mod 64 + M] Mod 64. These two results correspond to (P - Q) and (P - Q + M) respectively. Two cases need to be considered.

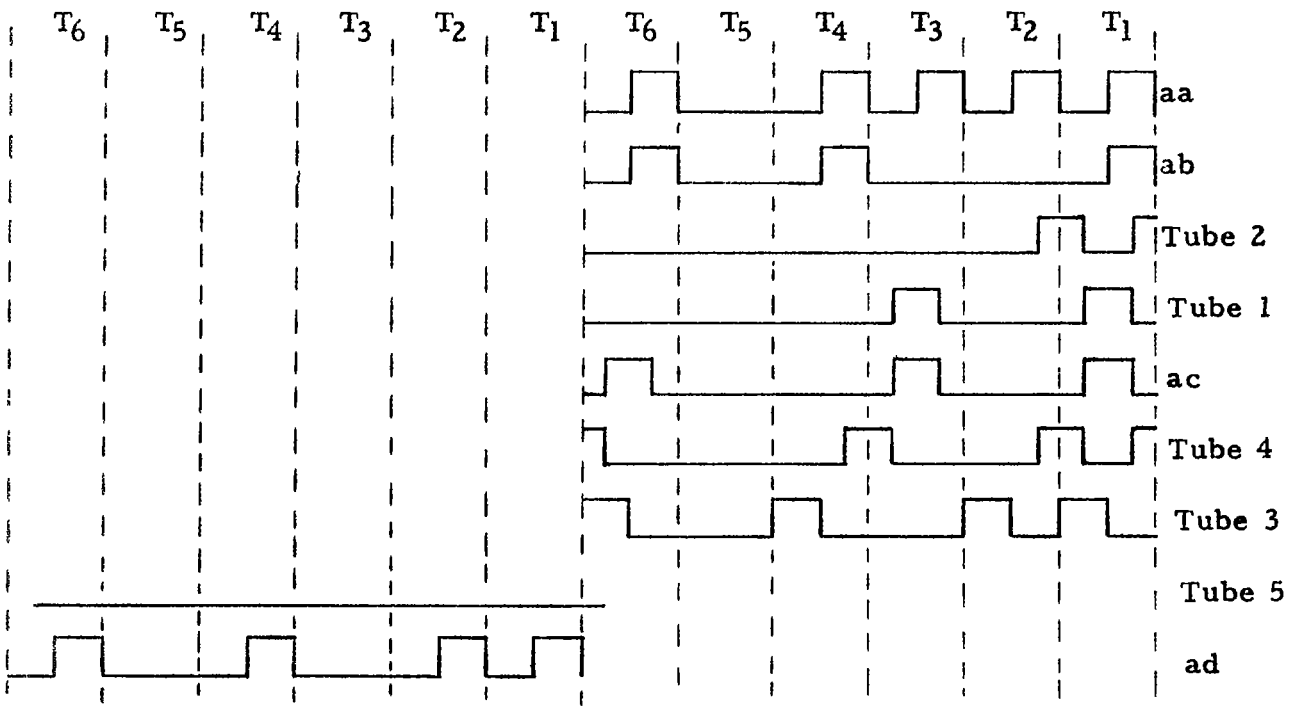
Case 1: $P \geqslant Q$

In this case the output of the subtractor is always positive and correct. A borrow can never be propagated beyond the 6th bit position and the result thus formed will be (P - Q). This is added to M in the adder to form a second and incorrect result (P - Q + M) Mod 64. The indication for controling tube 5 to select the correct result is provided by the condition of borrow over the end in the subtractor only. Therefore, when $P \geqslant Q$, tube 5 is always enabled at the ${}_3T_6$ sampling time and will be ON for the following six microseconds so that tube 6 uses the result from the subtractor to supply as the output. The following sketch shows pulse patterns for P = 18, Q = 16 and M = 26:



Case 2: $P < Q$

In this case the result formed in the subtractor is negative and incorrect. A borrow is always propagated past the 6th bit position which causes tube 5 to be OFF for 6 microseconds following the ${}_3T_6$ sampling time thereby selecting the result formed in the adder for tube 6 to supply as an output. The first result, (P - Q) Mod 64, is added to the modulus in the adder to form the correct result, [(P- Q) Mod 64 + M] Mod 64, which in effect (P - Q + M). For example, assume P = 16, Q = 22 and M = 26. The subtractor produces (16 - 22) Mod 64 = 58 and the adder produces (58 + 26) Mod 64 = 20. The following sketch shows pulse patterns for P = 16, Q = 22 and M = 26.



C. Absolute Differencing (P - Q), (Q - P)

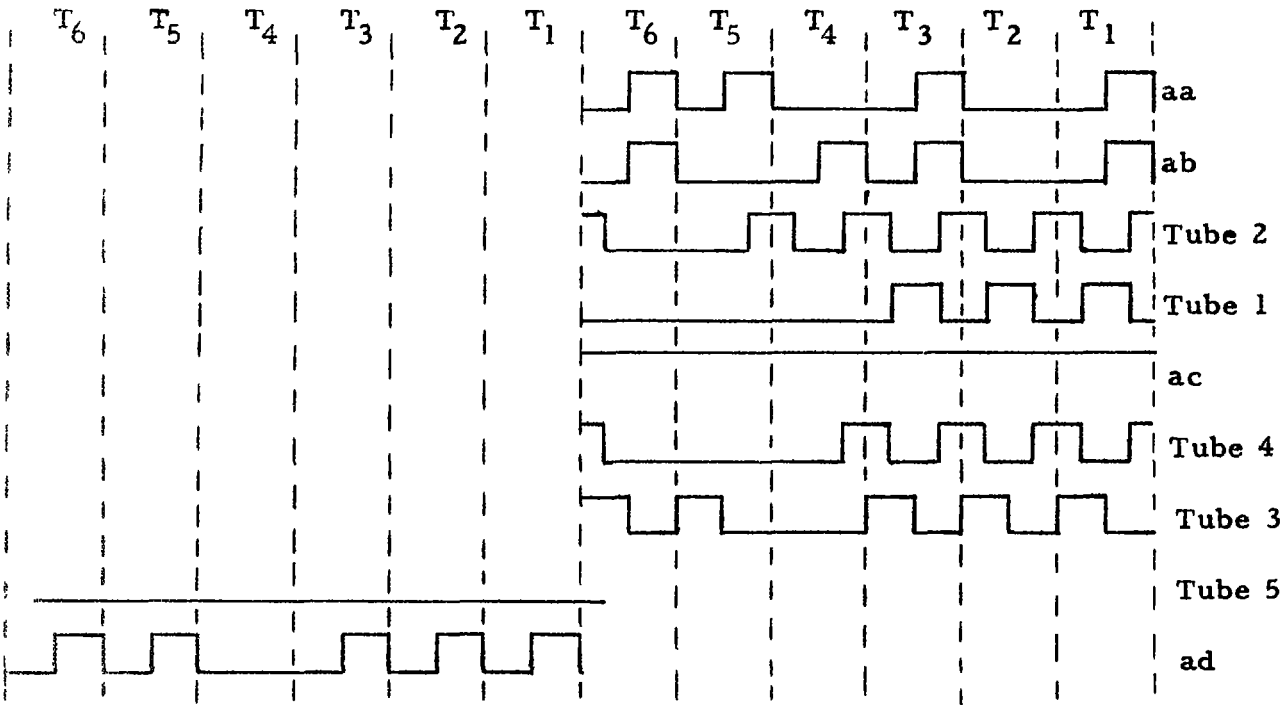
For this function the appropriate selection of the plug-in delay sticks or links must be made according to Notes 1, 2 and 3 on the logical diagram and a modulus of zero must be used. The first section functions as a Mod 64 subtractor, and the second section functions as a 2's complementer. When tube 4 is ON, the complementing rule for tube 3 is: 0 = 0 and 1 = 1. When tube 4 is OFF, the rule is: 0 = 1 and 1 = 0. Tube 4 is turned on at the beginning of the cycle and stays on until tube 3 puts out a blank, or no pulse, and then it turns off for the rest of the 6 microsecond cycle. Since the desired result may be either (P - Q) or (Q - P), two cases need to be considered:

Case 1: $P \geq Q$

In this case the subtractor forms the correct result (P - Q) just as it did in Case 1 for modular subtraction. The indication to control tube 5 is also the same as in subtraction and since no borrow can be propagated past the 6th bit position, the result formed by the subtractor is selected for tube 6 to supply as the output.

Case 2: $P < Q$

In this case the subtractor forms the incorrect result (P - Q + 64) and a borrow is propagated past the 6th bit position just same as in Case 2 for modular subtraction. The 2's complementer forms the correct result $[(64 - (P - Q + 64)] = 64 - P + Q - 64 = (Q - P)$ and because the subtractor propagated a borrow over the end tube 5 is caused to be in the off condition so the result from tube 3 is selected for tube 6 to supply as the output. The following sketch shows pulse patterns for P = 10 and Q = 18:



V. Physical Characteristics

Four complete and separate Mod-Adders are built on one plug-in chassis with all the input and output leads available on the two plugs at the back of the chassis. The four units are functionally independent but are interconnected

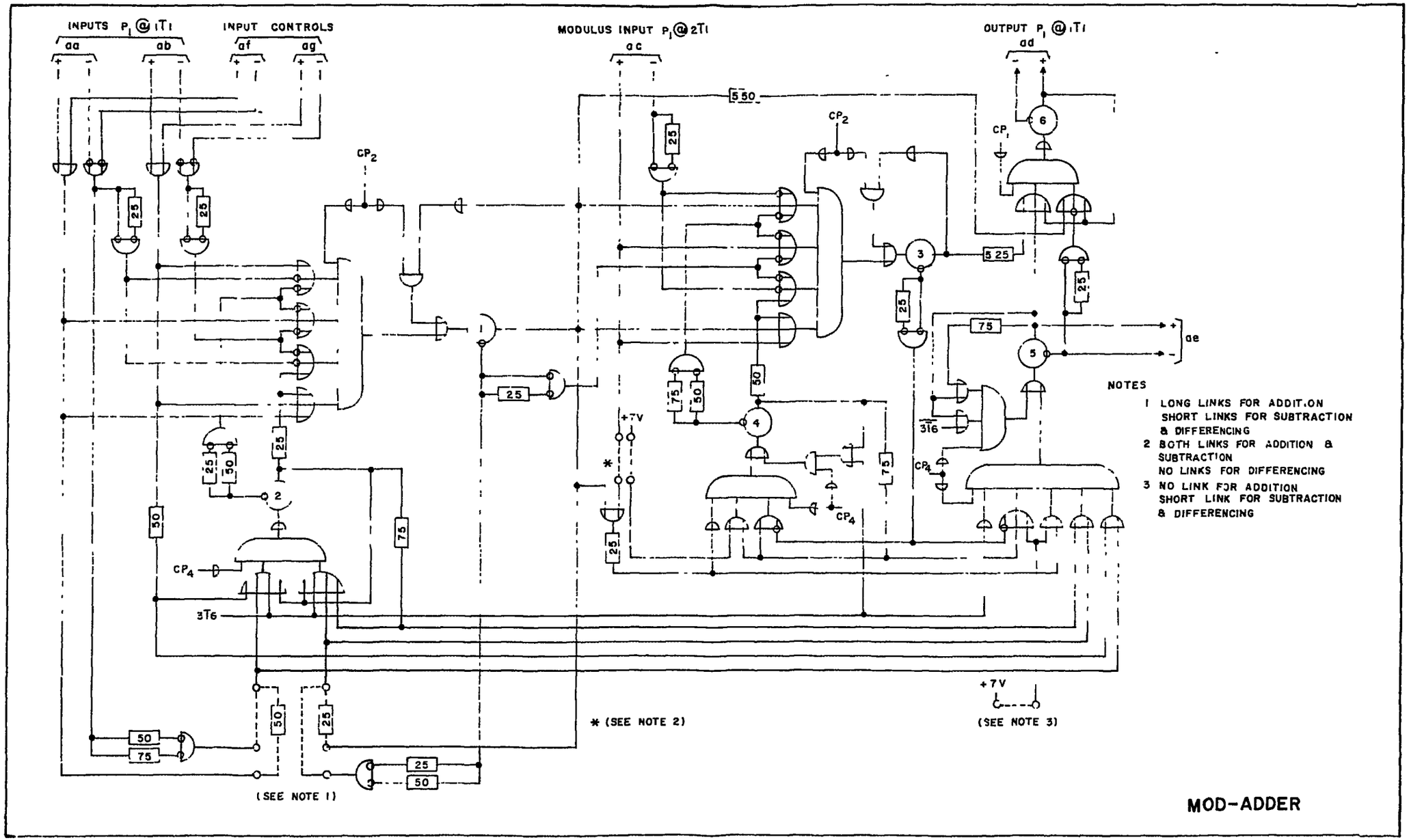
electrically. The circuit component requirement for one chassis of four Mod-Adders is approximately as follows:

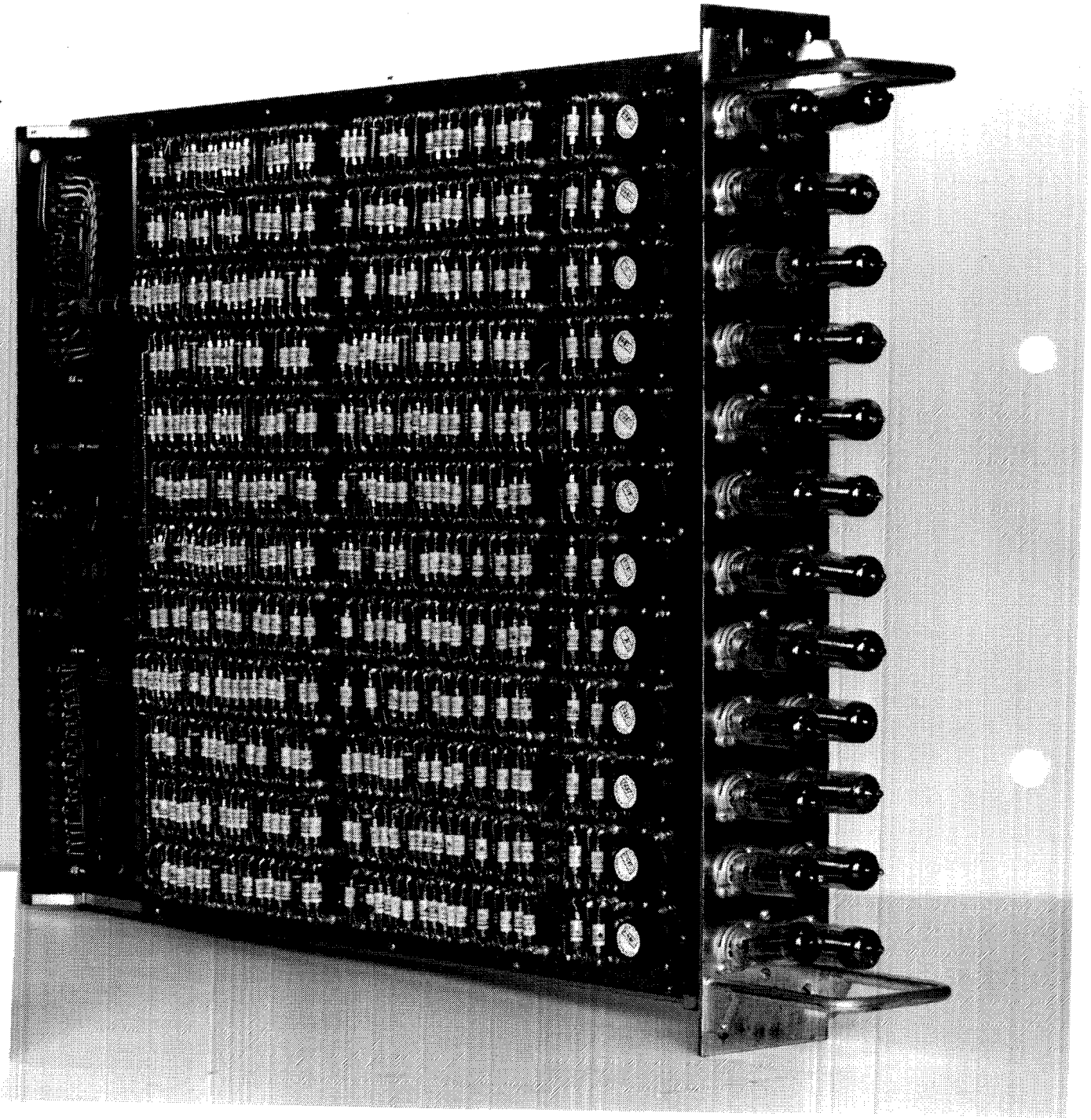
Vacuum tubes:	24 type 6AN5.
Pulse transformers:	24 plug-in ferrite type.
Crystal diodes:	820 type 1N34, CK705, or comparable type.
Delay lines:	140 sticks of one microsecond or fraction.
Resistors:	468
Filament transformer:	1 Thordarson type T21F12.

An average approximation of the power consumption on the more important voltages is as follows:

	Current	Watts
+200 V.	0.48 amp.	96
+62 V.	0.84 amp.	52
-8 V.	-0.7 amp.	-5.6
-65 V.	1.04 amp.	68
110 V. a-c	0.65 amp.	72

The total power dissipation is approximately 300 to 320 watts which represents a heat dissipation of 17 to 18 B.T.U. per minute.





M.A.

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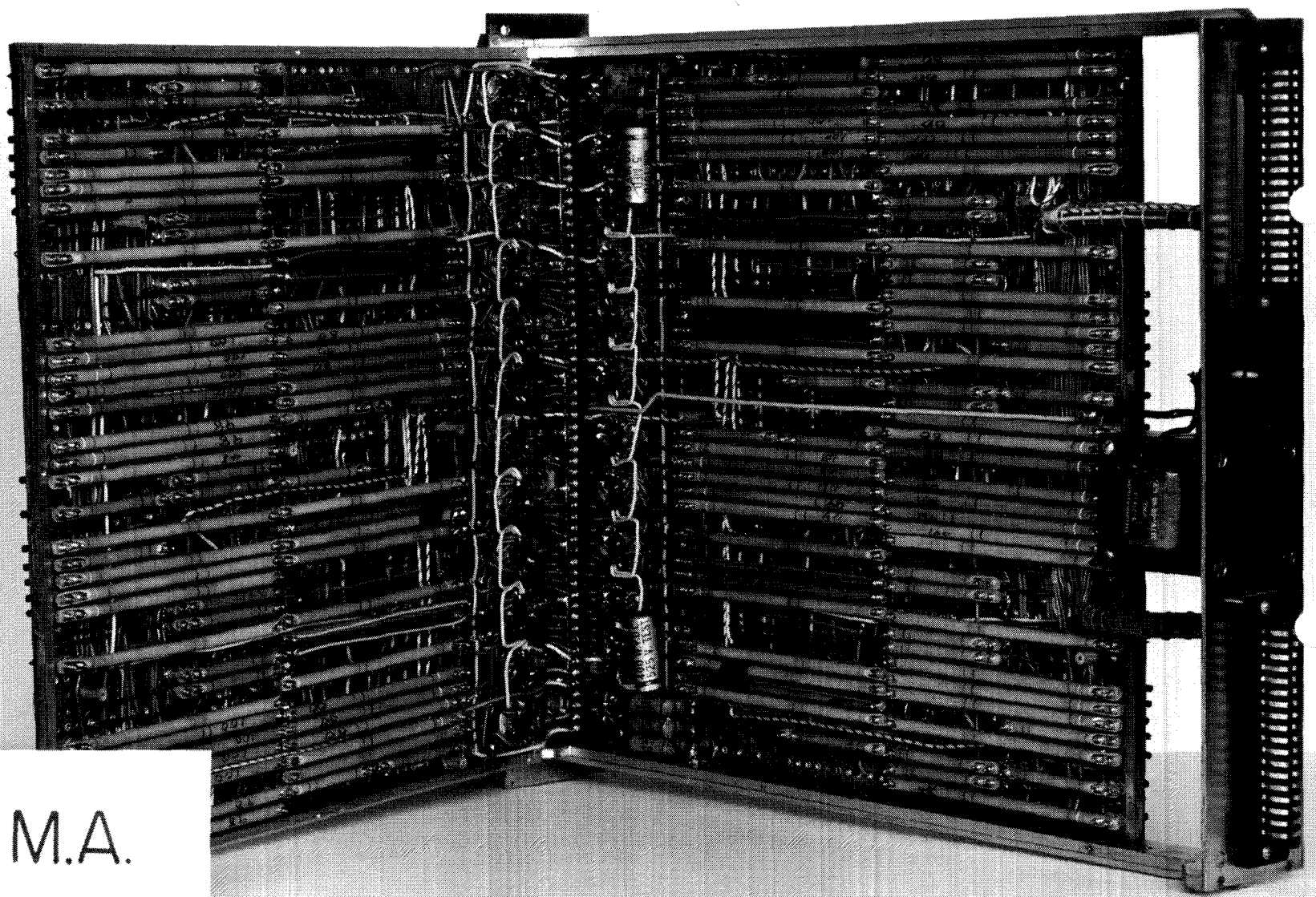

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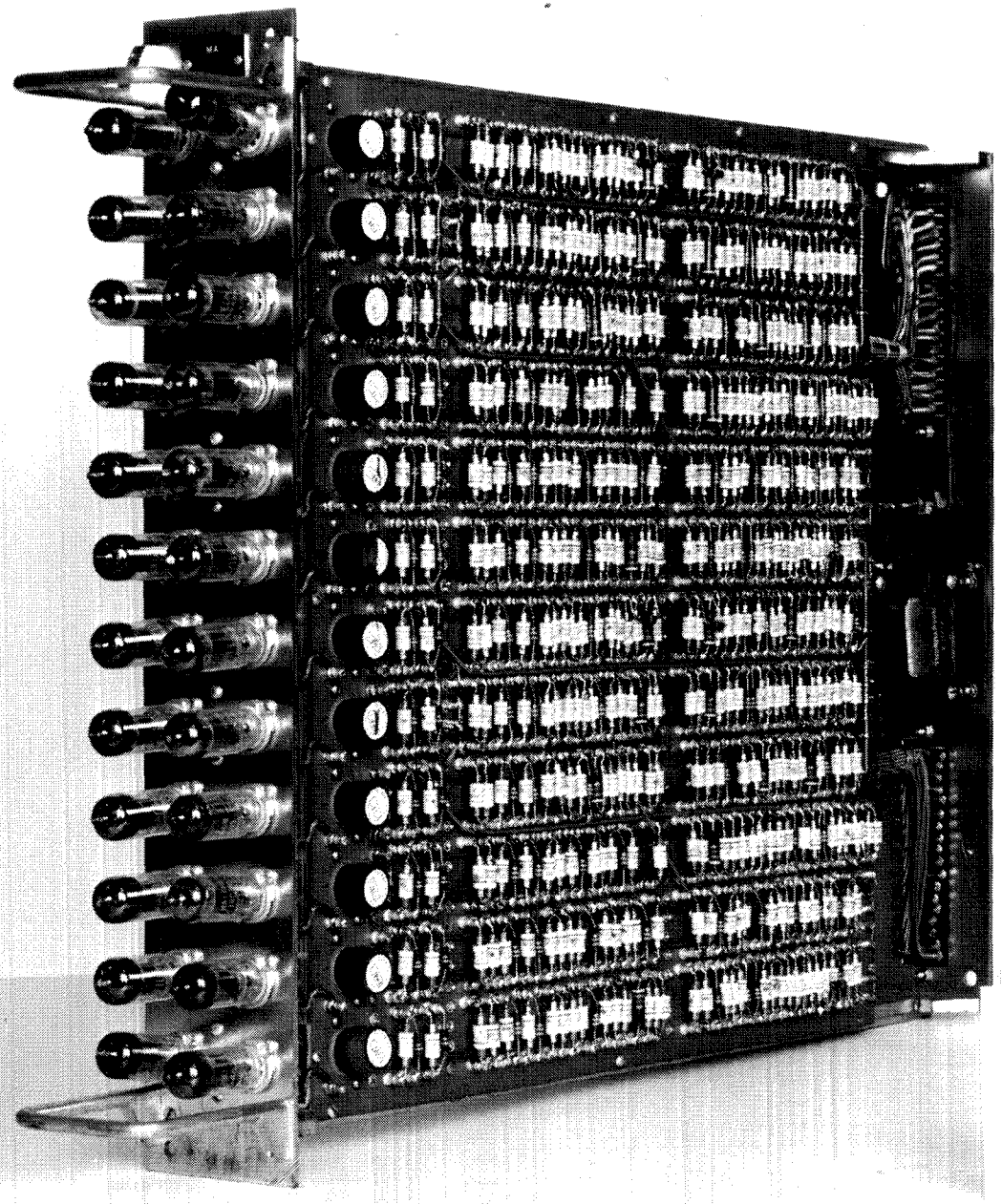


M.A.

CHAPTER 6

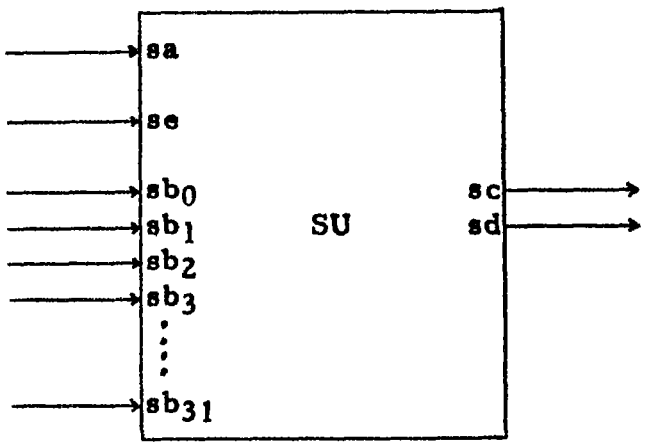
THE SUBSTITUTION UNIT (SU)

I. Function

The function of the Substitution Unit is to substitute one of 32 values, or 5-bit patterns, for another. This is accomplished at the rate of 167,000 per second. The relationship between the pattern fed into the unit and the substituted pattern is purely arbitrary and can be changed either automatically with additional circuitry, or manually.

II. Symbolic Representation

The following sketch shows how the Substitution Unit may be represented in a block diagram:



The functions of the leads may be defined as follows:

sa - Input pattern for which substitution is to be made. Its timing of P_1 may be anytime in the range ${}_3T_6$ to ${}_3T_1$.

sb_0 to sb_{31} - Input patterns for substitution timed P_1 at ${}_1T_6$.

sc - Early output timed P_1 at ${}_3T_6$.

sd - Normal output timed P_1 at ${}_4T_6$ or P_1 at ${}_1T_1$.

se - Input control. May be timed anytime from P_1 at ${}_3T_6$ to ${}_3T_1$.

III. Application and Programming Considerations

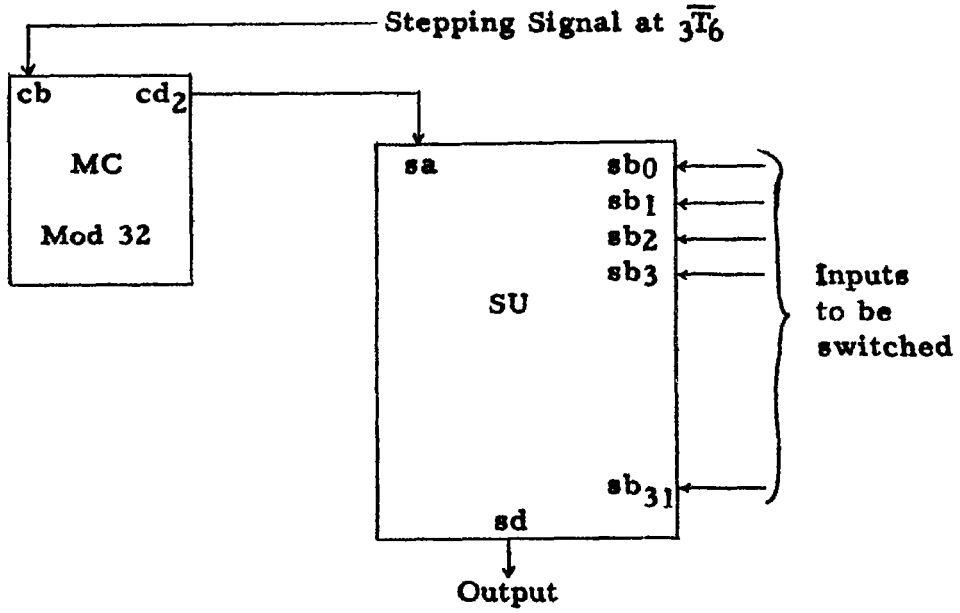
A. Simple Substitution

The primary purpose of the Substitution Unit is to provide a convenient means whereby one value or 5-bit pattern can be changed to or replaced by another. Three analytical uses of this type are (1) to represent the end-plate sequence of rotor cipher device, (2) to change from one 5-bit coding to another such as binary to letterwriter, etc., and (3) table look-up.

B. Selector Switch

1. With 32 positions or less

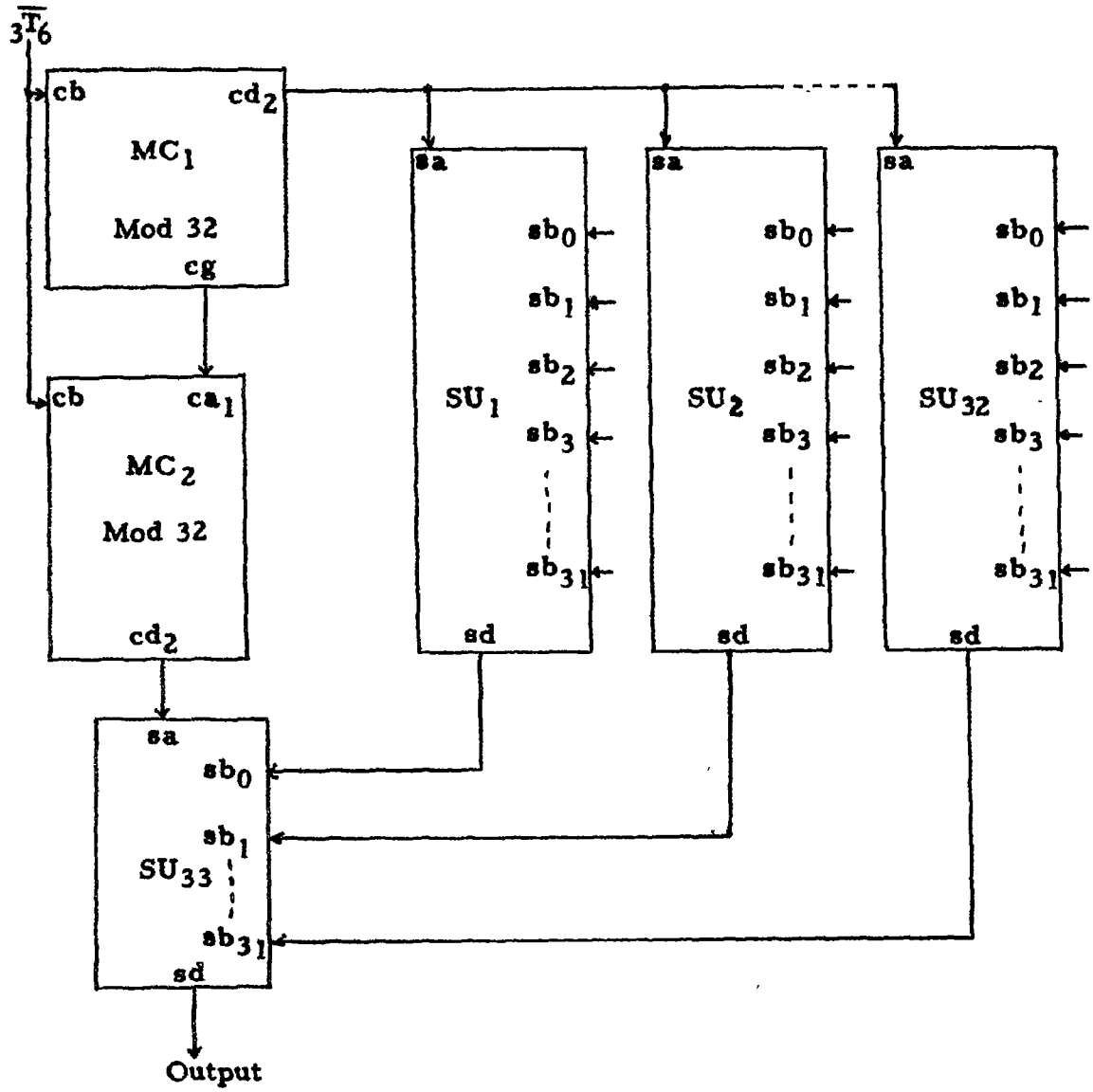
The Substitution Unit can be used as an electronic selector switch with up to 32 positions capable of being switched from one position to any other position in 6 microseconds. One simple means of accomplishing sequential switching is to supply the input from a Mod Counter as follows:



The Mod Counter supplies a sequence of numbers such as 0, 1, 2, 3, 4, 5, 6, 7, etc., to represent the position of the switch. The output of the Substitution Unit will be the pulse pattern on lead sb_0, sb_1, sb_2, sb_3, sb_4, sb_5, etc., corresponding to the respective switch positions. This is quite useful in cases where a fixed stream of data up to 32 elements is to be sequenced or scanned. Automatic homing can be accomplished from any position.

2. With many more than 32 positions.

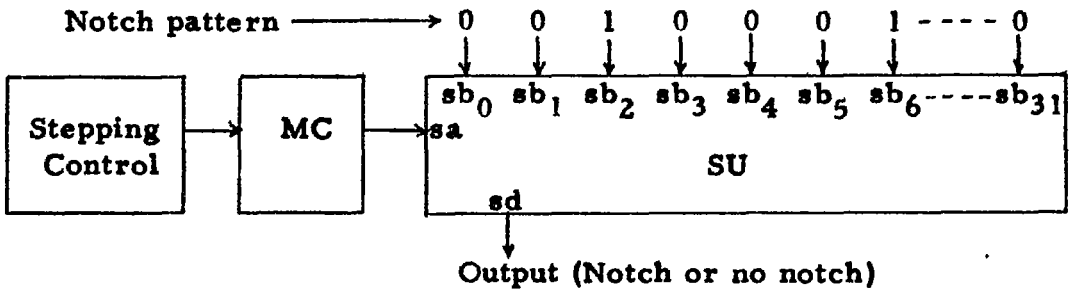
By using a cascade arrangement of 2 Mod Counters and up to 33 Substitution Units, an extra large electronic selector switch with as many as 1024 positions can be simulated. The following sketch shows a block diagram of such a switch:



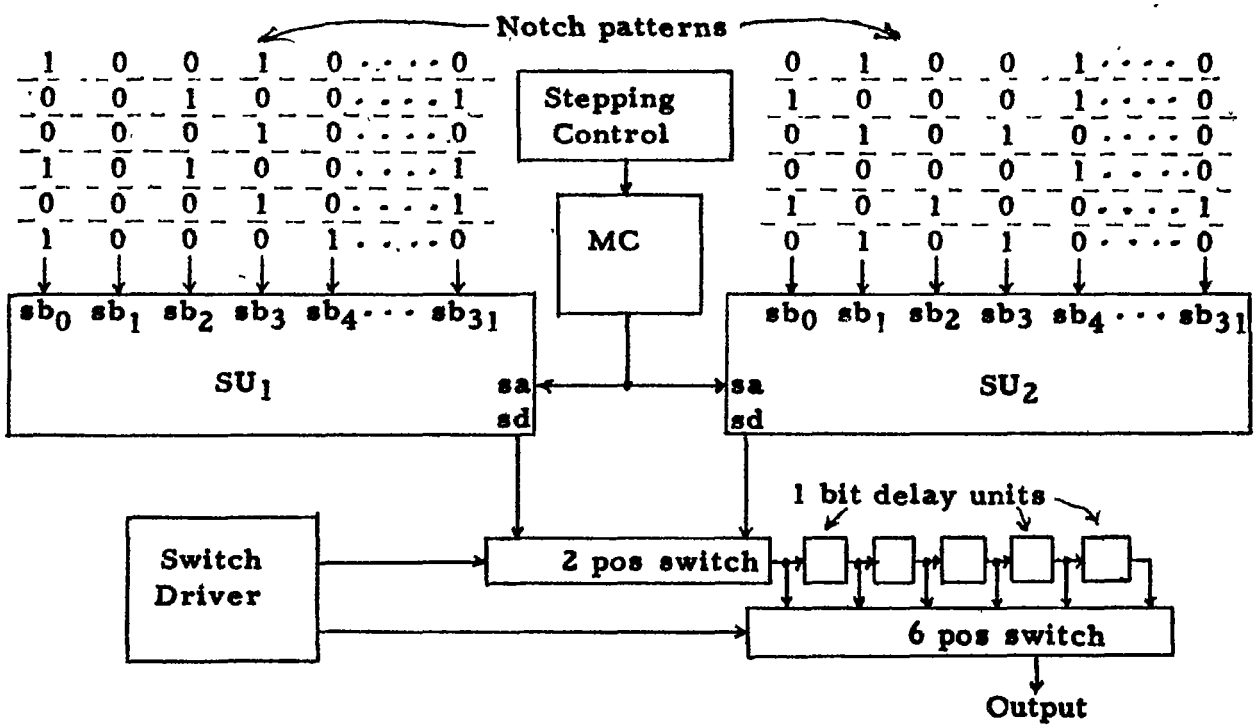
MC_2 keeps SU_{33} in one position while MC_1 drives SU_1, SU_2, SU_3, ... SU_{32} all through 32 positions. In this manner all 32 inputs to SU_1 can be switched in turn through SU_{33}. Then the 32 inputs to SU_2 are switched in turn through SU_{33}, etc., up through those of SU_{32}.

C. Rotor Notch Ring

The simulation of a rotor notch ring for controlling the stepping of other rotors is an item of major importance in an electronic representation of a rotor ensemble particularly in complex motions. There are several methods by which notch rings may be simulated when a set of rotors are stepped through a sequence of successive positions and the use of a Substitution Unit is just one of them. The following sketch is an example:



This scheme is not very economical but it does provide a rather flexible notch ring. With the addition of a 6-position time switch on the output as many as six notch rings can be applied to a rotor. The number of notch rings can be increased by the use of more Substitution Units and switches. An example showing up to 12 notch rings is given in this next sketch:



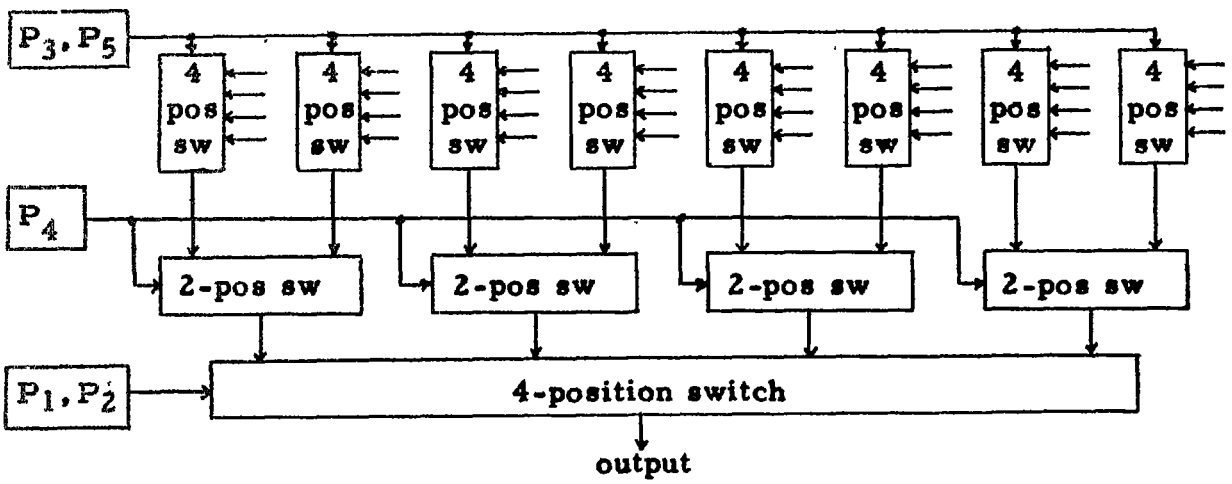
One notch ring is represented by the P_1 bits of the pulse patterns of SU_1, another by the P_2 bits, etc. The conditions of the 2-position and the 6-position switches determine which notch pattern is to be used.

IV. Operation

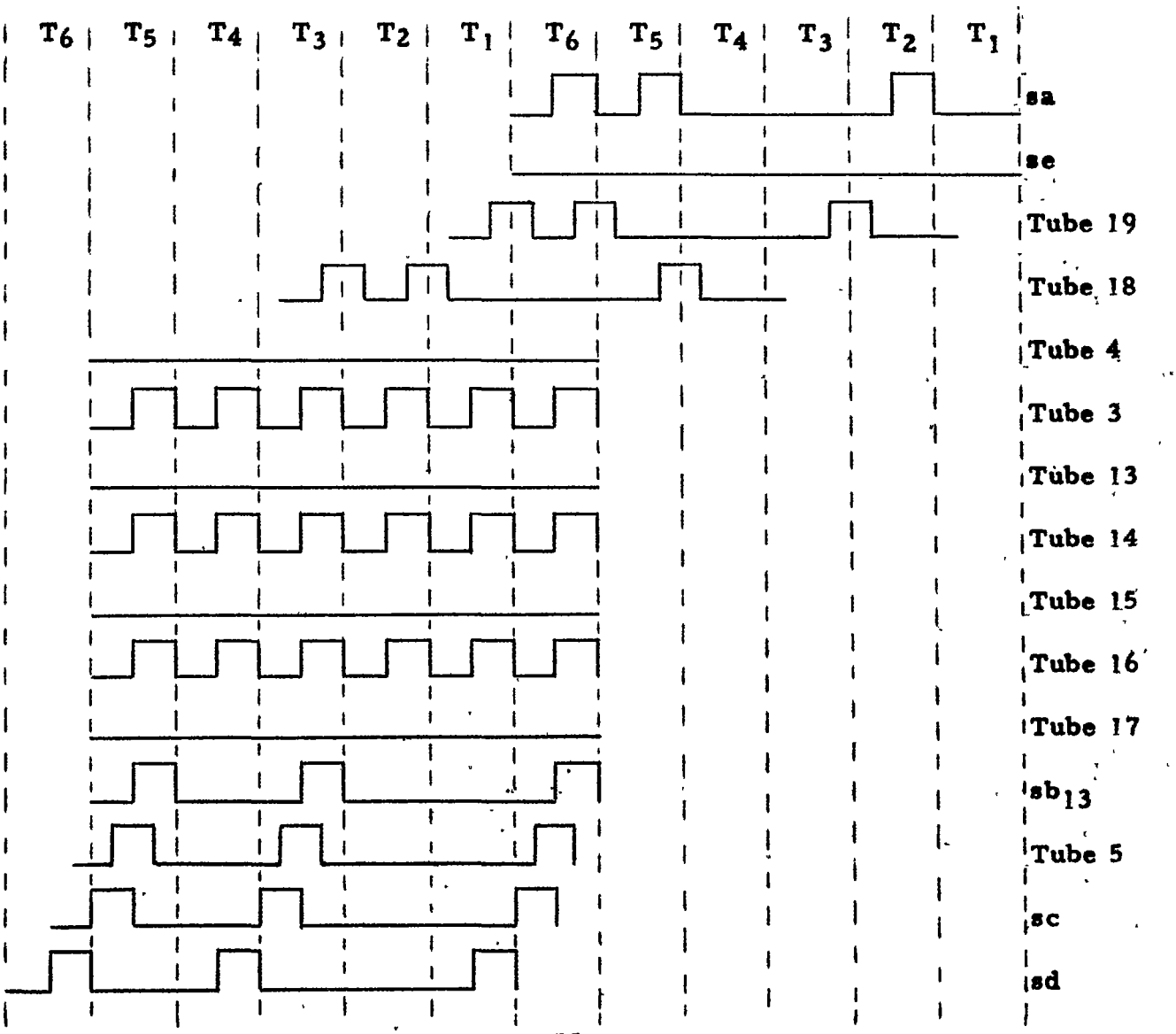
The operation of the Substitution Unit is based on a six microsecond time cycle. The input on lead sa occurs during one cycle and the output on lead sd occurs during the following cycle. Lead se is provided to permit an input control. When a continuous stream of pulses is on lead se, the signal on lead sa has no effect. When no pulses appear on lead se, the signal on lead sa controls the operation of the circuit. As an example, assume the value 13 is being replaced by 22.

The pulse pattern for the value 13 (13 = 10010) is fed in on lead sa in serial form and is held in tubes 18, 19 and associated delay lines until all five bits are received. The timing of the input may be as early as P_1 at $_3T_6$ requiring a 1.00 microsecond delay line or may be as late as P_1 at $_3T_1$ requiring no delay line. When all 5 bits of the input pattern have been received, they are used to appropriately set the selector drive flip-flops consisting of tubes 3, 4, 13, 14, 15, 16, and 17. Tubes 4, 3, 13, 15, and 16 are turned ON when pulses occur in positions P_1, P_2, P_3, P_4, and P_5 respectively. Tubes 14 and 17 (complements of tubes 13 and 16) turn ON when no pulses occur in positions P_3 and P_5, respectively. For the pattern representing 13 (10010) tubes 3, 14, and 16 are turned ON and tubes 4, 13, 15, and 17 are turned OFF.

The mechanism which selects 1 of 32 patterns for the output is divided into several parts which may be shown in functional block form as follows:



For circuit considerations each of the 2-position switches are combined with their two respective 4-position switches to form the gating structure for one tube. To follow the example further the 4-position switch associated with tube 2 lets through the signal from tube 5 when tube 4 is OFF and tube 3 is ON. When tube 14 is ON one of the "AND" gates of tube 5 is enabled and when tube 15 is OFF the other "AND" gate of tube 5 is not inhibited. The condition of tubes 4 and 3 determines the selection of 1 of 4 inputs for each of the "AND" gates of tubes 5, 7, 9 and 11. Therefore, input pattern 13 sets up the appropriate selection drivers to select the signal on lead sb_{13} for the output. This signal should be the pattern for 22 (01001) in order to satisfy the example. The following sketch shows pulse patterns at various points in the circuit for the above example:



V. Physical Characteristics

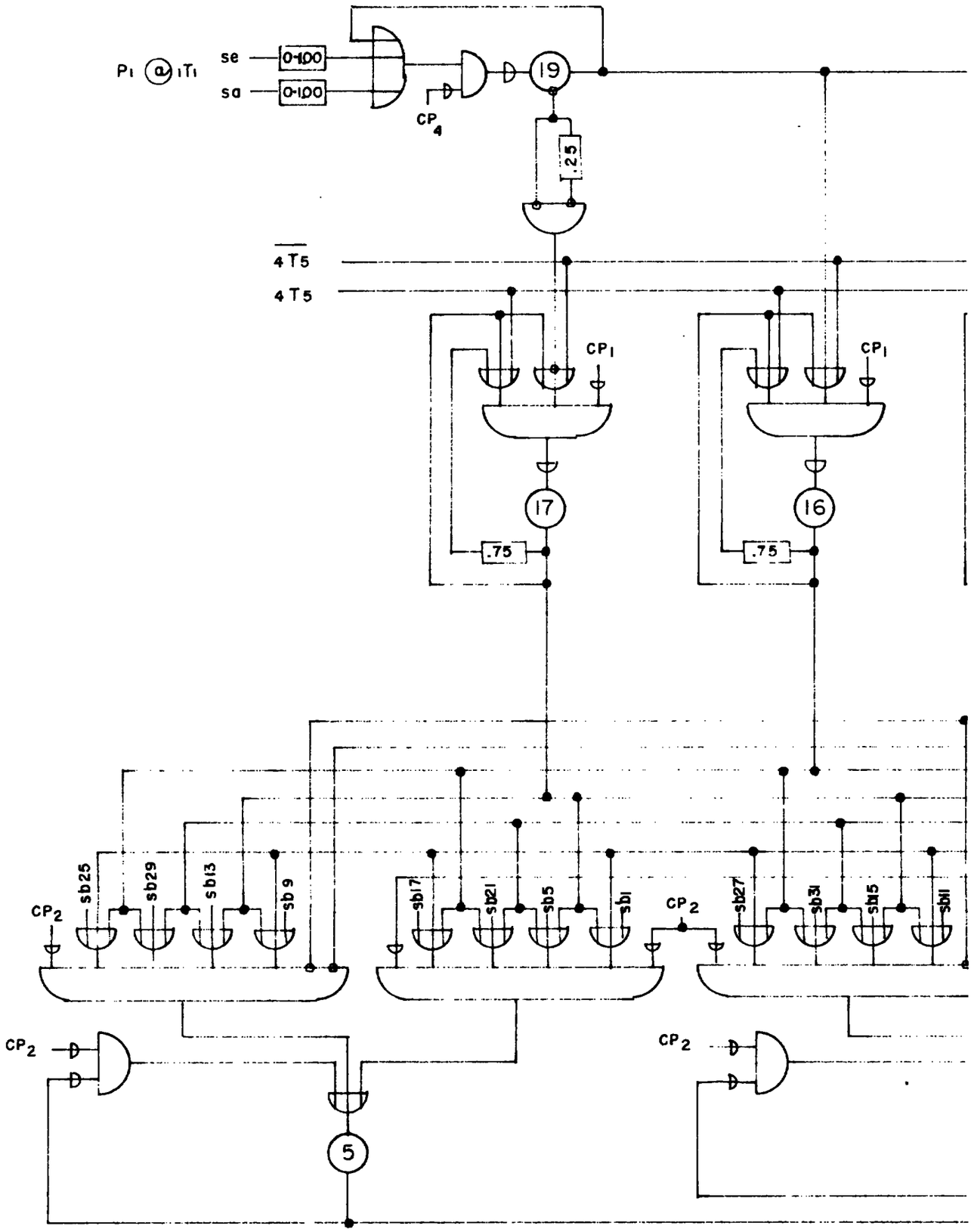
The Substitution Unit is built on one chassis with a little space to spare. All the input and output leads are available on the plugs at the back of the chassis. The circuit component requirement for one chassis is approximately as follows:

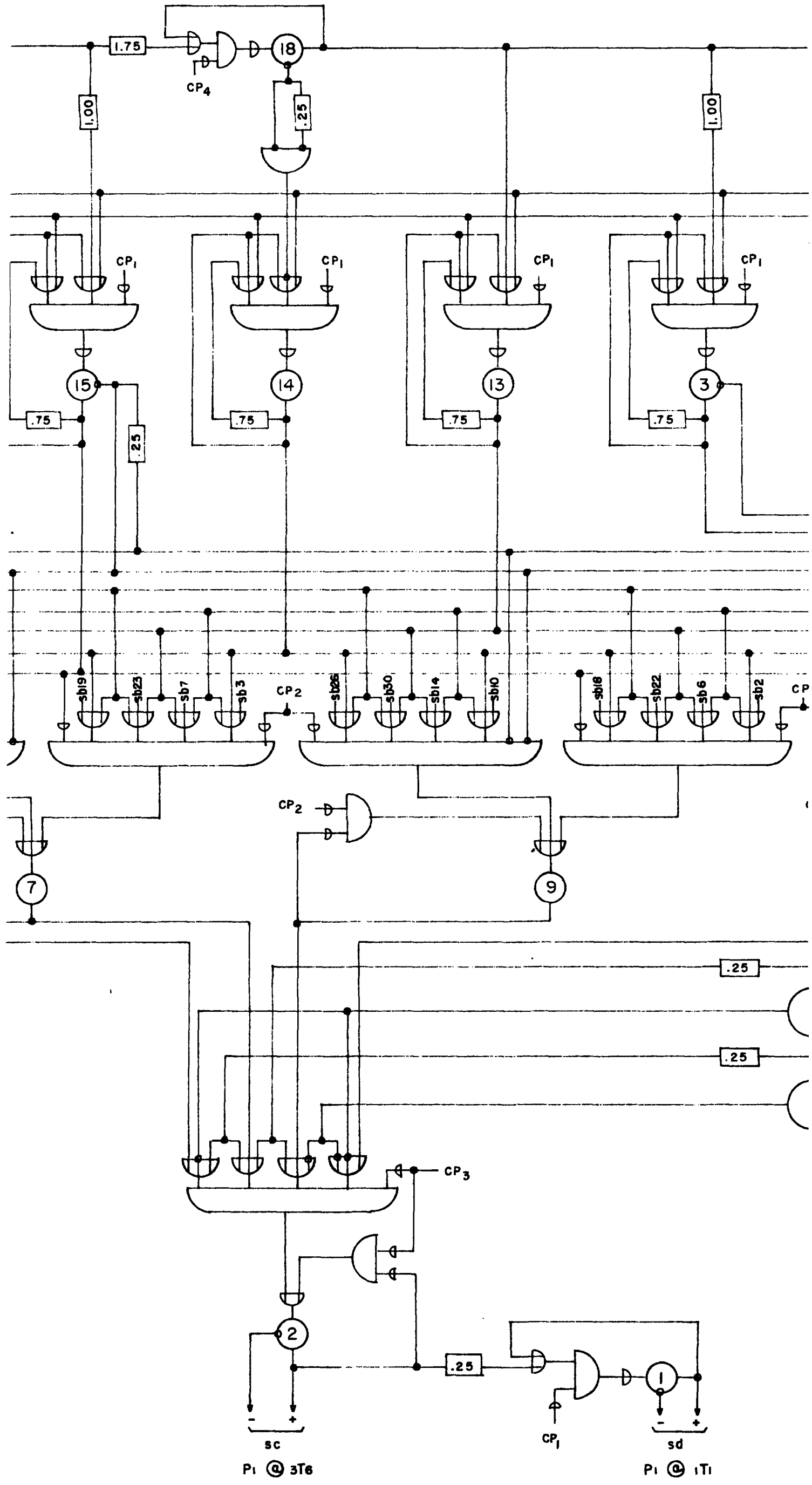
Vacuum tubes:	15 type 6AN5
Pulse transformers:	15 plug-in ferrite type
Crystal diodes:	377 Kemtron type 345
Delay lines:	24 sticks of 1 microsecond or fraction
Resistors:	188
Filament transformers:	1 type T21F12

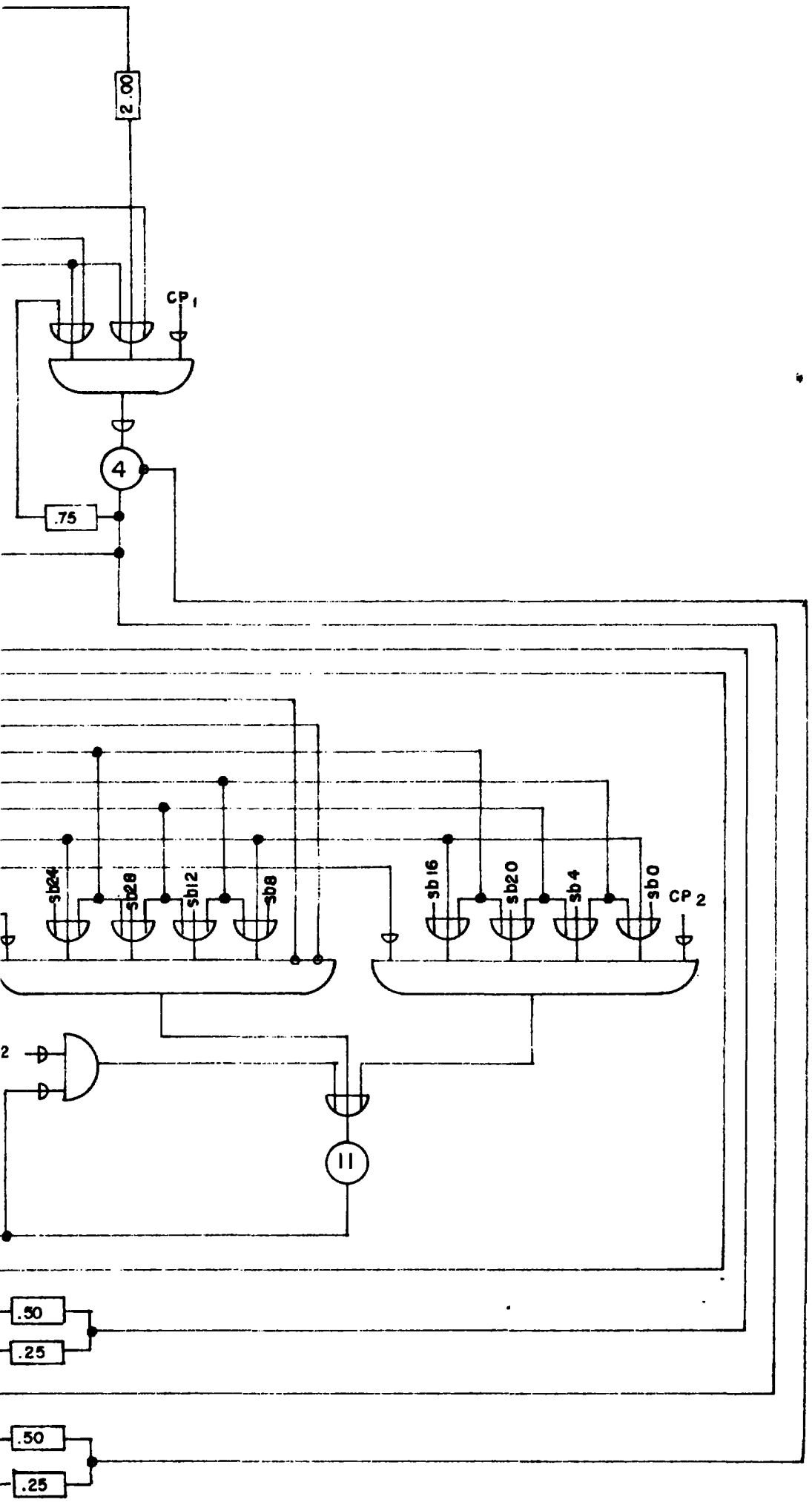
The approximate power requirement for the more important voltages is as follows:

	Current	Watts
+200 V.	.29 amps	58
+ 62 V.	.42 amps	26
- 8 V.	-.28 amps	- 2
- 65 V.	.9 amps	58
110 V. a.c.	.41 amps	45

The total power dissipation is approximately 189 to 205 watts which represents a heat dissipation of 10.7 to 11.6 B.T.U. per minute.







SUBSTITUTION UNIT

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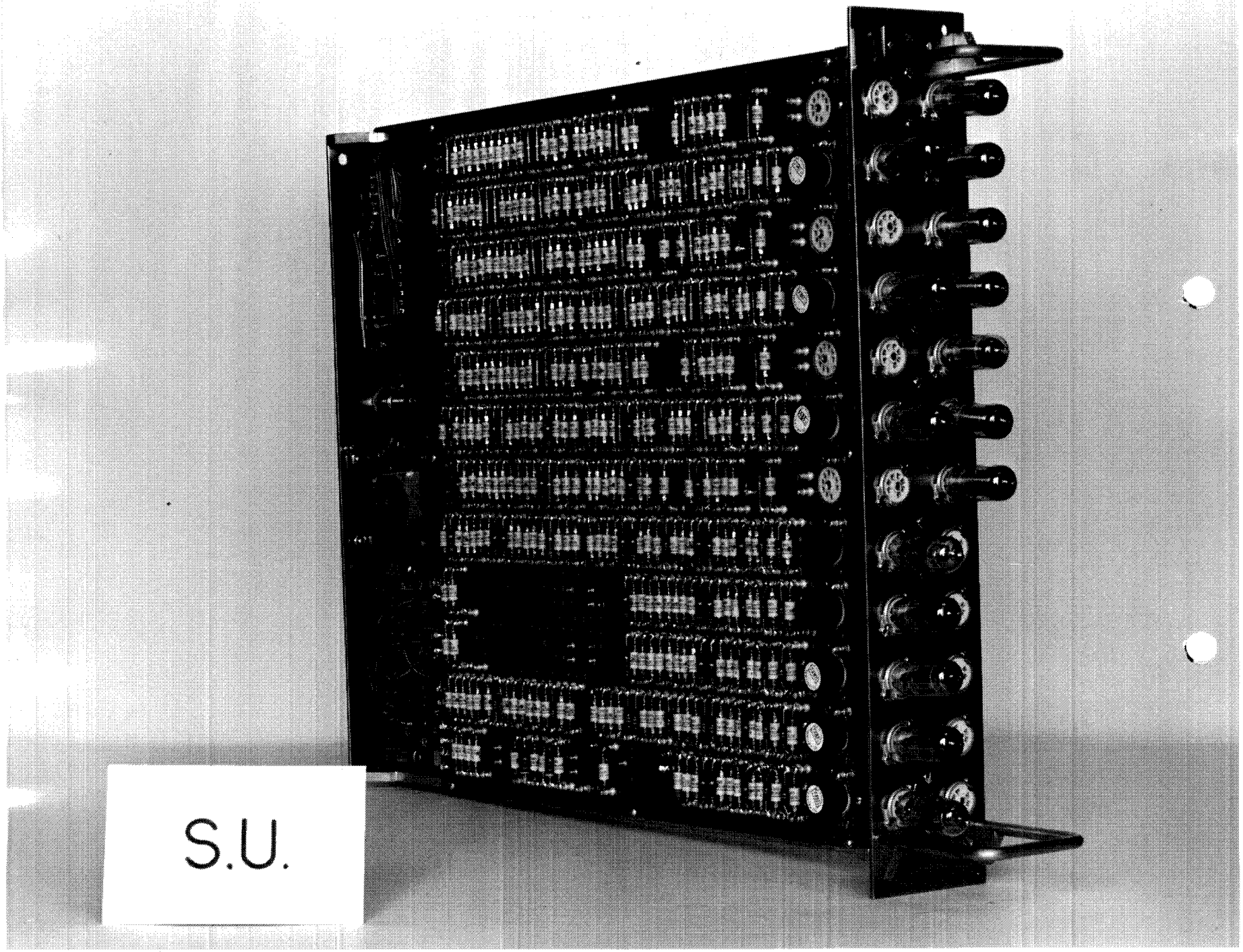

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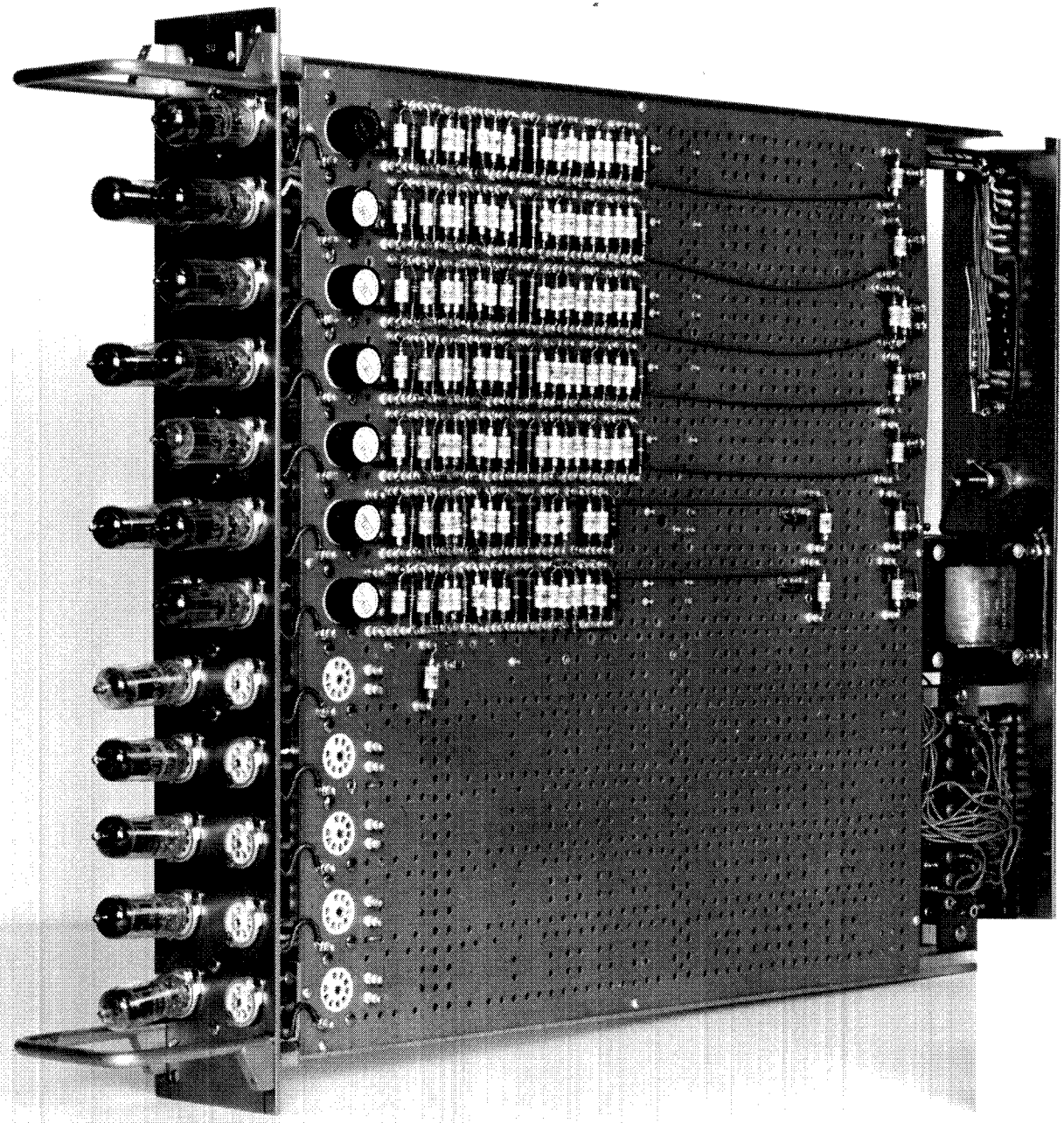

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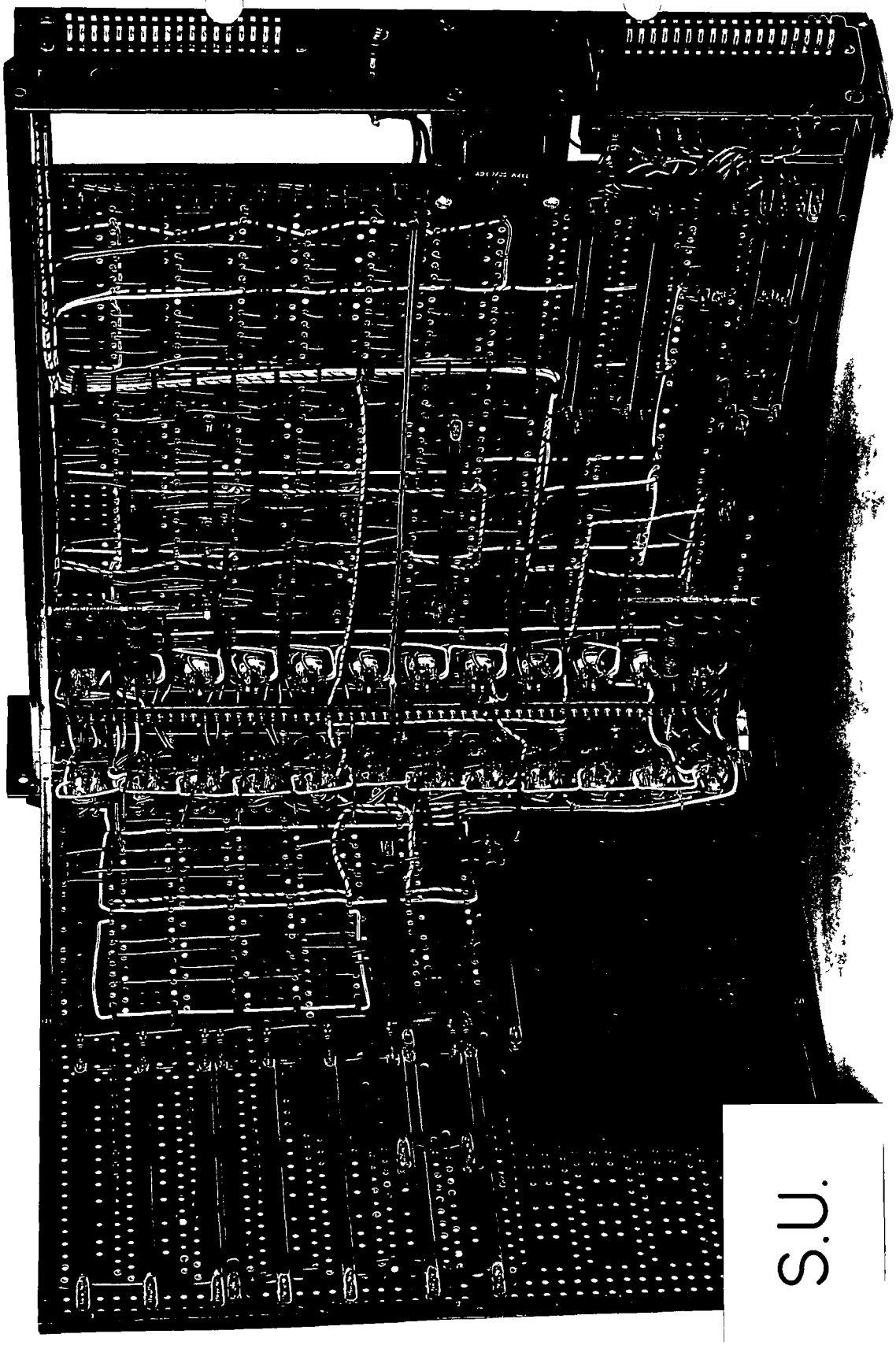

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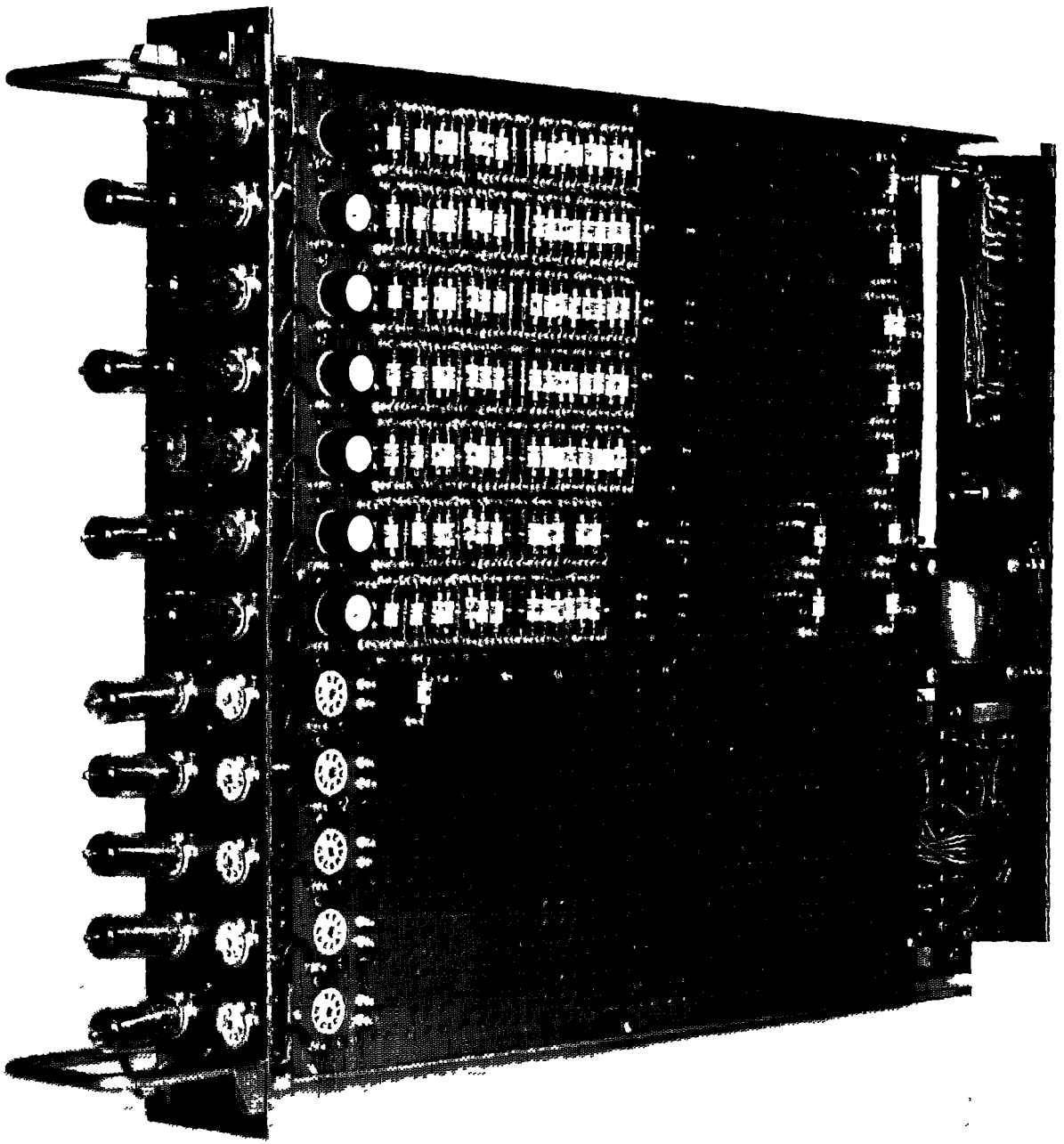

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CHAPTER 7

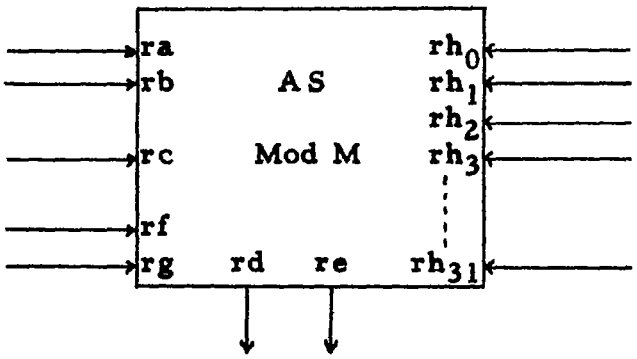
THE ADDER SELECTOR (AS)

I. Function

The primary function of the Adder Selector is that of representing a wired rotor which may have any number of points up to a maximum of 32. One limitation is that it is capable or processing only one letter at a time.

II. Symbolic Representation

The following sketch shows how the Adder Selector may be represented in a block diagram:



The functions of the leads may be defined as follows:

ra, rb - Input leads: These two leads are for the two primary input patterns one representing a letter and the other representing a rotor position. Both must be timed P_1 at ${}_1T_1$.

rc - Modulus input timed P_1 at ${}_2T_1$.

rd - Early output timed P_1 at ${}_3T_6$.

re - Normal output timed P_1 at ${}_1T_1$.

rf, rg - Input controls: These two leads are provided to permit control of the inputs on leads ra and rb respectively. The pulse patterns on these leads must be timed P_1 at ${}_1T_1$.

rh_0 to rh_{31} - Pattern leads timed P_1 at ${}_1T_6$. These leads provide 32 inputs which represent the rotor output points.

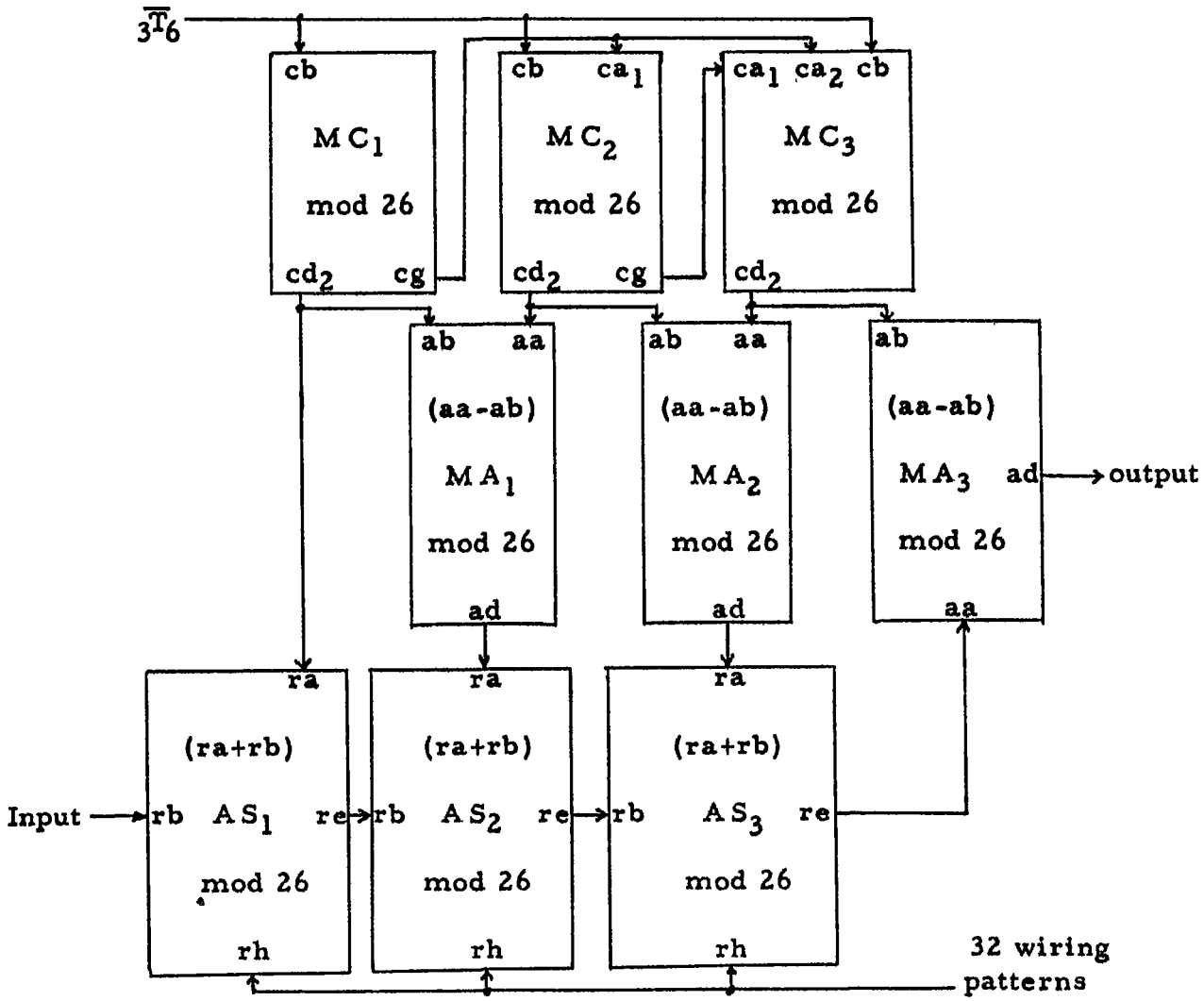
III. Application and Programming

The Adder Selector was designed to perform electronically the functions of a wired rotor in the encipherment or decipherment of a letter. This is accomplished by the modular addition of two quantities, one representing the input letter and the other representing the displacement of the rotor with respect to its endplate or preceding rotor, and using that sum to perform a table look-up or a substitution function to derive the output letter. These two steps can be performed separately by the use of a Mod Adder described in Chapter 5 and a Substitution Unit described in Chapter 6 each of which requires a 6-microsecond cycle, whereas, the Adder Selector requires only one 6-microsecond cycle. Therefore, in function the Adder Selector combines the capabilities of a Mod Adder and a Substitution Unit into one unit and one character cycle. The descriptions of the above two units also apply generally to the Adder Selector so will not be repeated here, but an attempt is made to describe the process of representing a wired rotor.

The operation of a wired rotor can be envisioned as a substitution table in which the table index represents the input points and the values put into the table represent the output points. For example, assume a 26-point rotor with input points rh_0 through rh_{25} arranged consecutively around the rotor which serve as a table index and the pulse pattern fed into each of these inputs represents the corresponding output point wired to that input point. Assume further that this rotor is adjacent to an endplate with a regular sequence of inputs 0-25 around it and that both the rotor and endplate are in position 0 with respect to a point in space. The adder portion of the Adder Selector must operate with a modulus of 26 to do modular addition, or subtraction, depending on which way the rotor moves. With the rotor at position 0 its input point is the same as the exit point of the endplate. If the rotor is moved N positions from 0 its input point is also moved N position with respect to the endplate, therefore, the letter must be added to, or subtracted from, by an amount equal to the distance the rotor has moved from 0. One input to the adder represents the output of the endplate and the other input represents the position of the rotor with respect to the endplate. The result of the addition or subtraction which now represents the actual input point to the rotor is used to select one of the leads rh_0 through rh_{25} on which is a pattern of pulses representing the output letter for that corresponding input letter. The selected output letter is now ready to pass through an endplate but must be corrected by modular subtraction, or addition, due to the fact that the output points of the rotor have been moved in space by the same amount as the input points. If, however, the output letter of one rotor is to be utilized as the input letter for another it does not have to be modified but the rotor position indication for the second rotor must represent the relative position of the second rotor with respect to the first.

For fixed wiring, fixed pulse patterns from a pattern generator referred to in Chapter 1 may be used to feed the rh leads. A plugging arrangement on the chassis itself is provided so that the actual wiring may be plugged up manually within the chassis. For non-fixed wiring which is to be changed electronically the source of the patterns for the rh leads should be from one character storage delay or other circuit elements whose patterns are a result of prior analytical tests.

Several rotors may be represented by several Adder Selectors in cascade. It takes one character cycle for one letter to go through one rotor in serial fashion, therefore, N rotors will consume N character cycles. By the use of Mod Counters and Mod Adders to generate rotor positions and Adder Selectors to serve as the wired rotors an arrangement of three 26-point rotors utilizing a metric motion is demonstrated in the following sketch:



In the foregoing example, it must be assumed that the endplate sequences are arranged in the same direction as the rotor points and that the rotor steps in such a manner that its successive positions will be in ascending order. The two blocks labeled [1D] and [3D] represent 1-character and 3-character delays respectively. MC_1, MC_2, and MC_3 generate the absolute positions of the three rotors; MA_1 derives the relative position of rotor 2 with respect to rotor 1; MA_2 derives the relative position of rotor 3 with respect to rotor 2; AS_1, AS_2 and AS_3 represent rotors 1, 2 and 3; and MA_3 derives the endplate output from the position of rotor 3 and its output letter. One cycle of delay is consumed in each rotor and one cycle in MA_3 so the output is exactly four cycles or 24 microseconds later than the input. If the output endplate had a plugging arrangement, another Adder Selector would have been needed instead of MA_3 and the same time would have been consumed.

Changes in the wiring of rotors can be made in as little as 6 microseconds or up to 32 x 6 microseconds or more depending upon which gives the best time-equipment economy.

IV. Operation

The operation of the adder portion is identical to that of the Mod Adder described in Chapter 4 with three exceptions. It works on 5 bits rather than 6; instead of one output it provides both the corrected and uncorrected outputs from tubes 15 and 13 respectively; and the carry indicator, tube 17, puts out a single pulse or no-pulse timed at ${}_4T_6$ instead of a set of 6 pulses or 6 no-pulses.

The operation of the selector, or substitution portion, is identical to that of the Substitution Unit described in Chapter 6 with three exceptions. It does not have an input control; two inputs, the corrected and uncorrected sums are stored in electrical delay lines; and the output of tube 17 is used to determine which 5-bit result is stored on flip flops. Tube 17 puts out a pulse at ${}_4T_5$ in all cases where the sum is less than the modulus. If a carry bit is produced or propagated past the 5th bit is either of the two addition steps tube 17 puts out no pulse at ${}_4T_5$. When the quantities 9 and 5 are added Mod 26 the result is 14 which is less than the modulus, therefore, tube 17 produced a pulse at ${}_4T_5$ to determine the fact that the right result 14 from tube 13 should be stored in the selector driver tubes (4, 3, 24, 23, 22, 21, 20) instead of the wrong result [9+5+(32-26)] mod 32 = 20 from tube 15. When the sum of two quantities is greater than the modulus tube 17 puts out no pulse at ${}_4T_5$ to determine the fact that the result from tube 15 is correct. An example of this is the addition of (21+25) mod 26 where the first result is (21+25)-32=14 and the second result is [(21+25)-32+(32-26)] mod 32 = 20.

V. Physical Characteristics

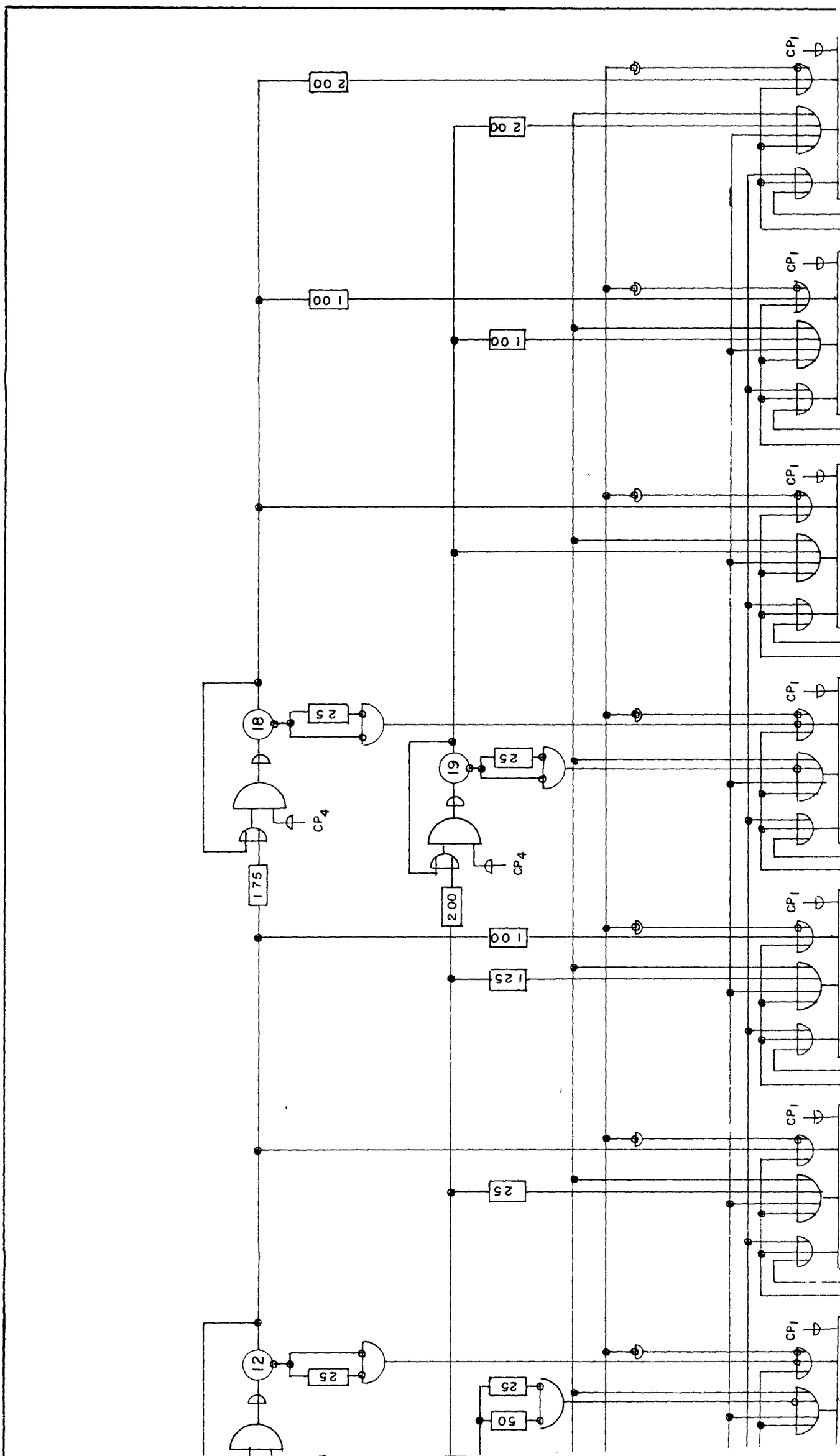
One Adder Selector completely fills one chassis with an approximate circuit component requirement as follows:

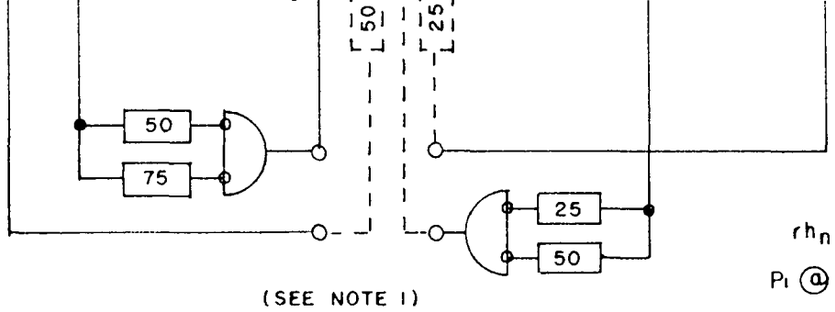
Vacuum tubes:	21 type 6AN5
Pulse transformers:	21 plug-in ferrite type
Crystal diodes:	700 type IN34, CK705, or comparable type
Delay lines:	73 sticks of one microsecond or fraction
Resistors:	343
Filament transformer:	1 Thordarson type T21512

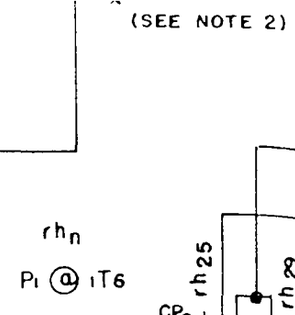
The power consumption on the more important voltages for one chassis is approximately as follows:

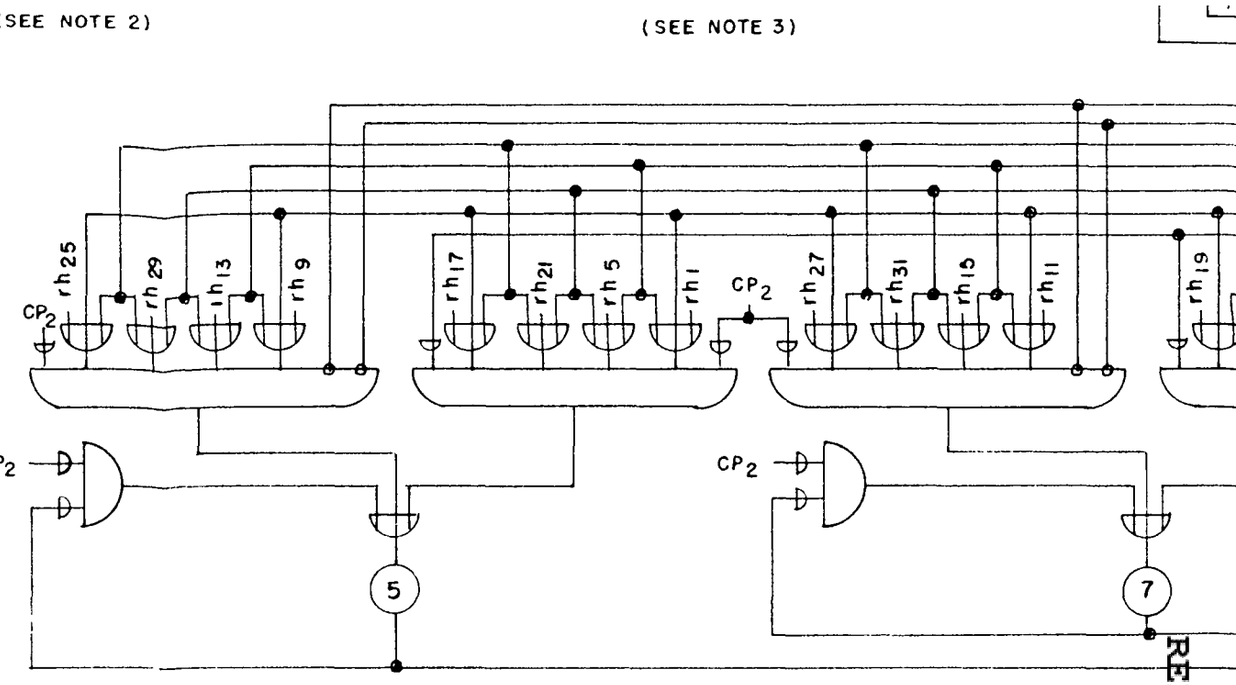
	Current	Watts
+200 V.	0.42 amp.	84
+62 V.	0.66 amp.	41
-8 V.	-0.95 amp.	-7.6
-65 V.	1.28 amp.	83
110 V. ac	0.58 amp.	63

The total power consumption is approximately 270 to 280 watts which represents a heat dissipation of 15 to 16 B.T.U. per minute.









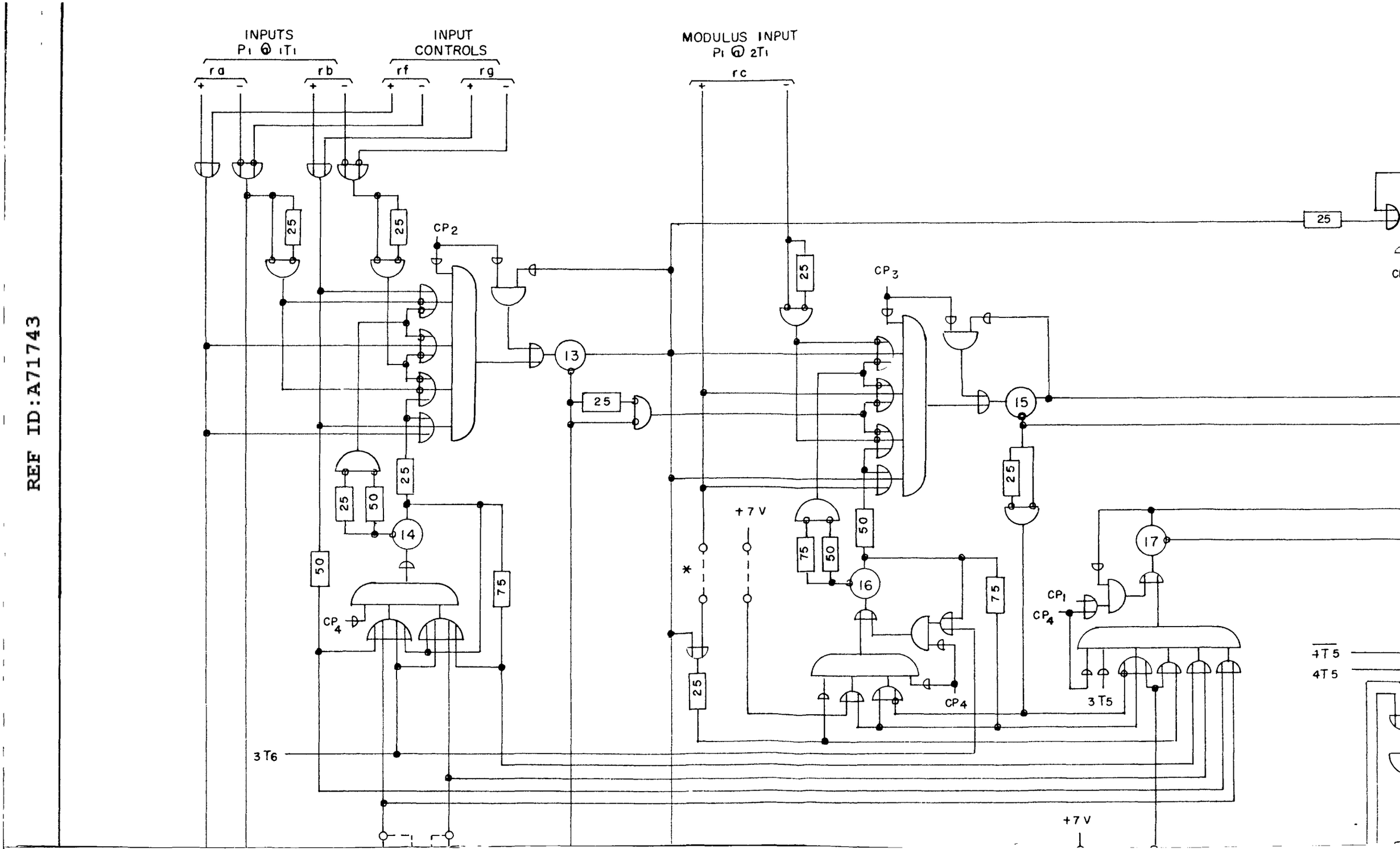
NOTE

1 LONG LINKS FOR ADDITION
SHORT LINKS FOR SUBTRACTION AND DIFFERENCING

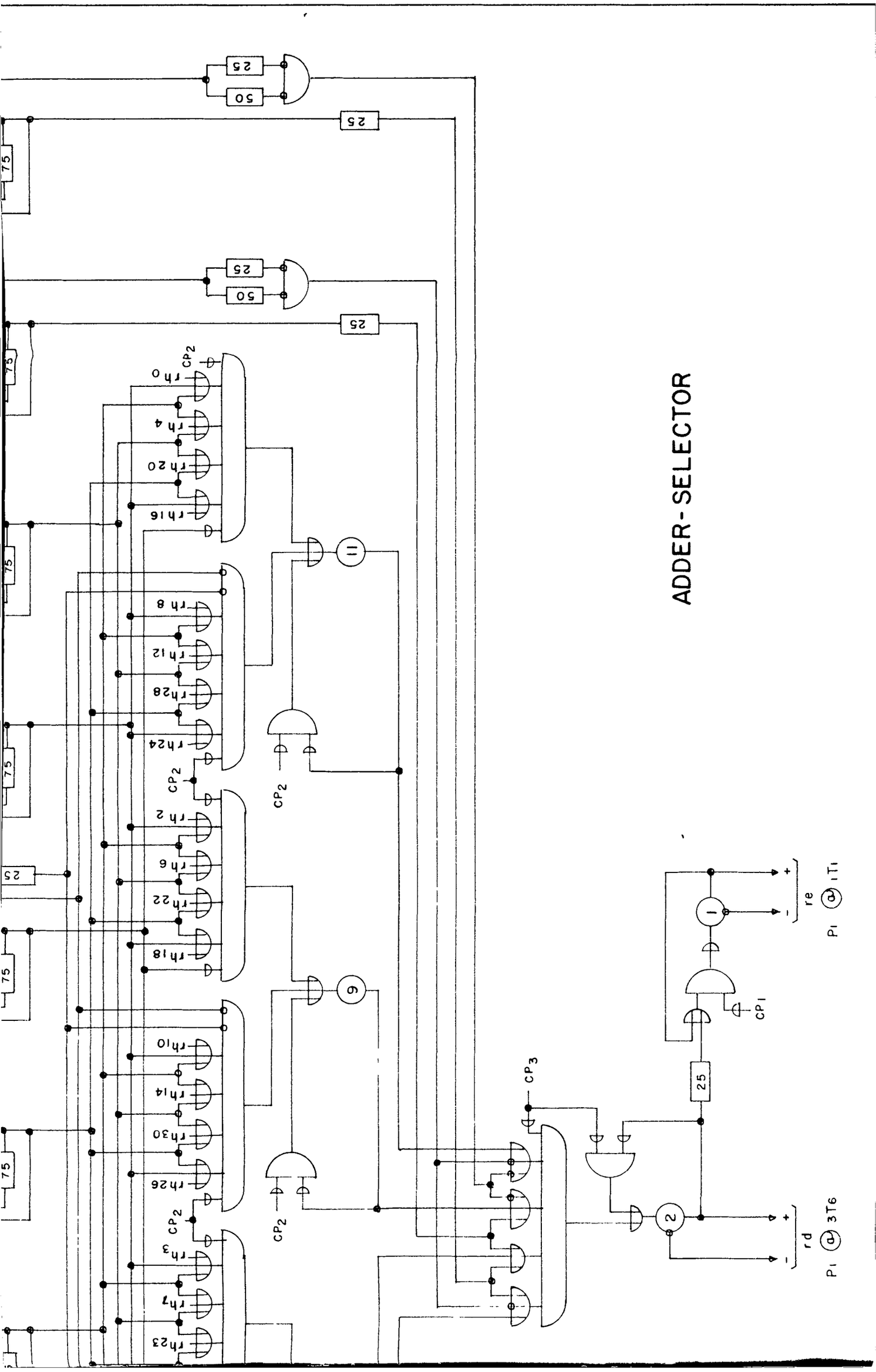
2 BOTH LINKS FOR ADDITION AND SUBTRACTION
NO LINKS FOR DIFFERENCING

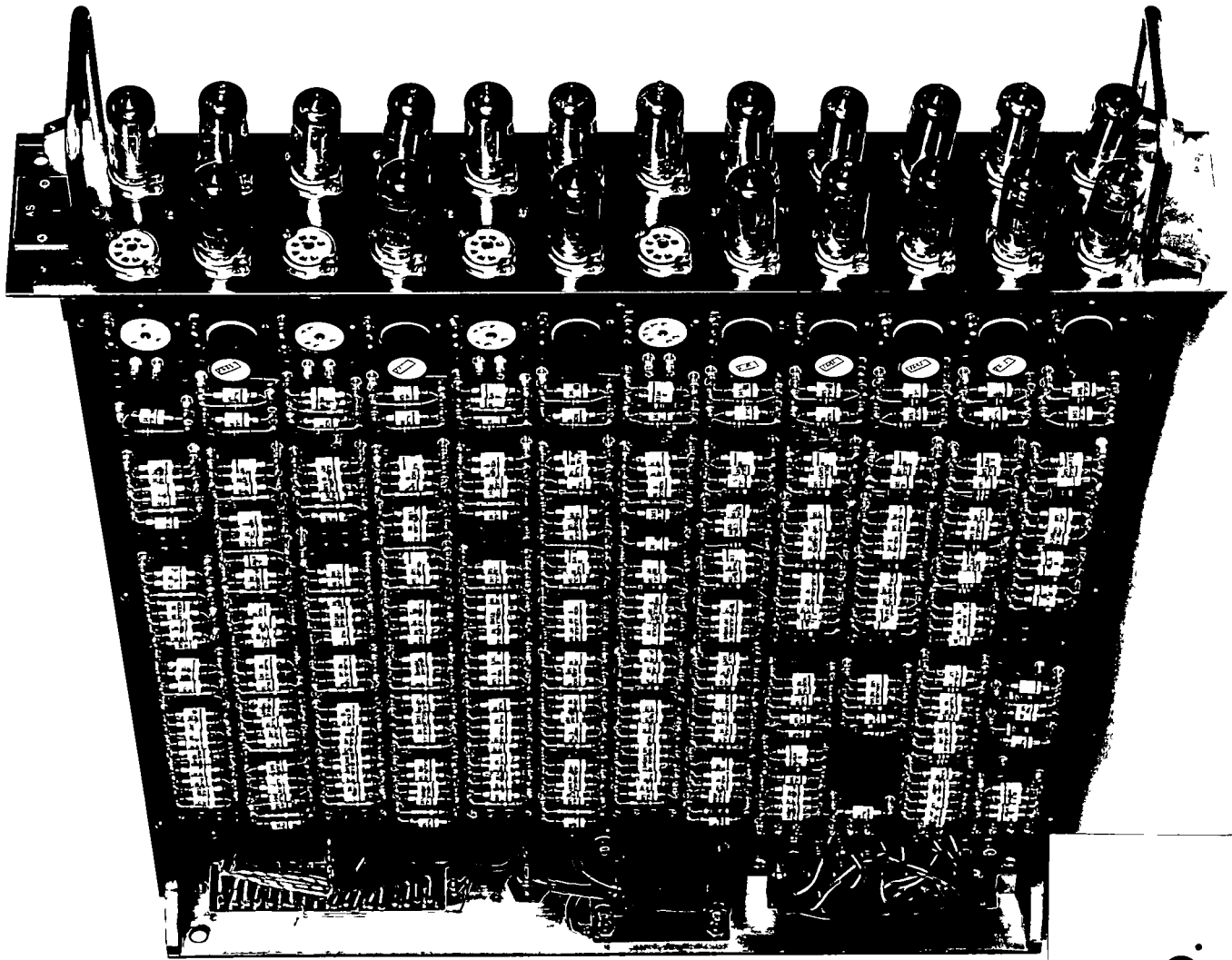
3 NO LINK FOR ADDITION
SHORT LINK FOR SUBTRACTION AND DIFFERENCING

REF ID:A71743

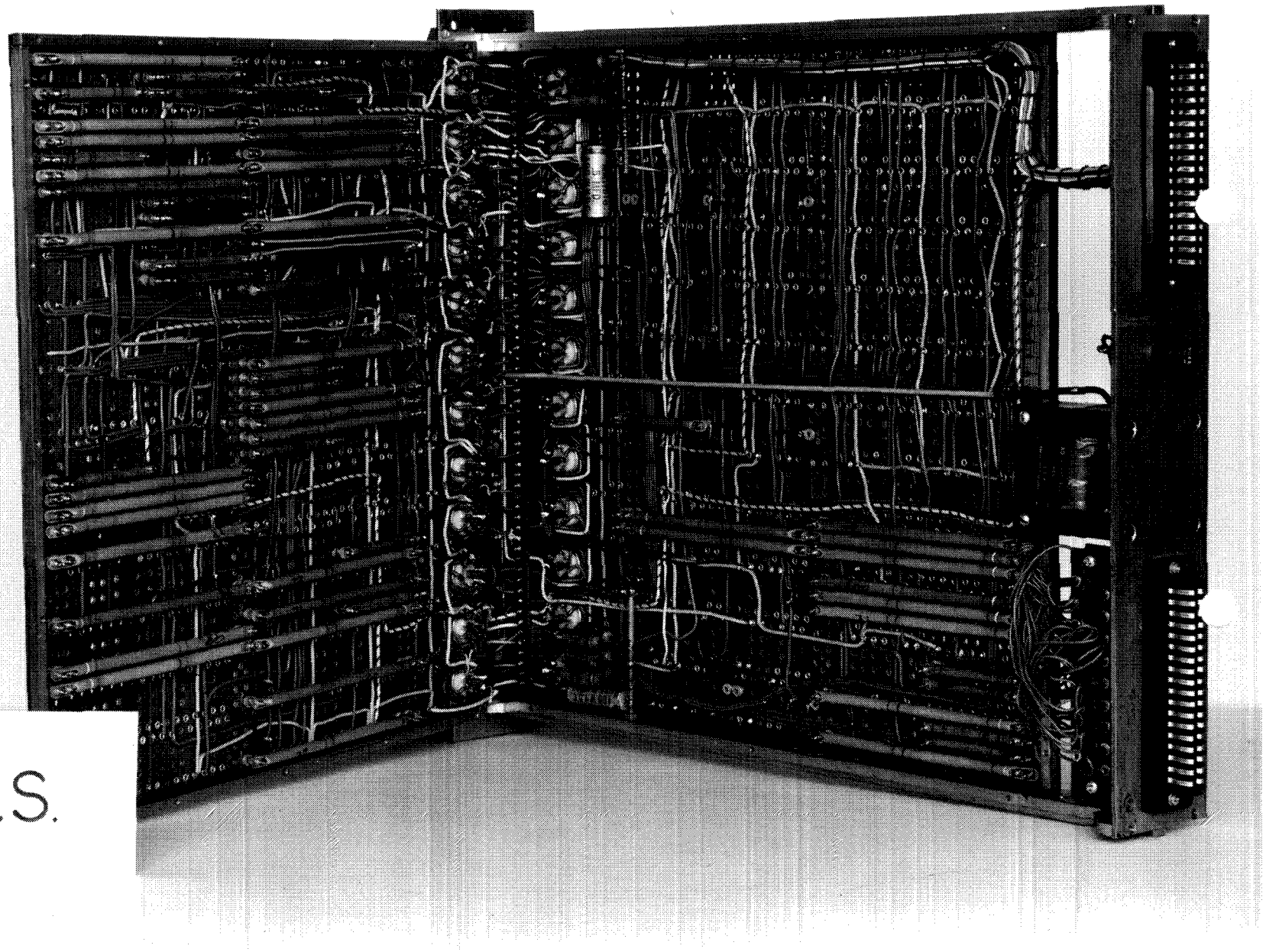


REF ID:A71743


ADDER-SELECTOR
25
50
75
CP2
CP3
CP1
rh 0
rh 4
rh 20
rh 16
rh 8
rh 12
rh 28
rh 24
rh 2
rh 6
rh 22
rh 18
rh 10
rh 14
rh 30
rh 26
rh 3
rh 7
rh 23
11
6
2
1
re
rd
P1 @ 1T1
P1 @ 3T6

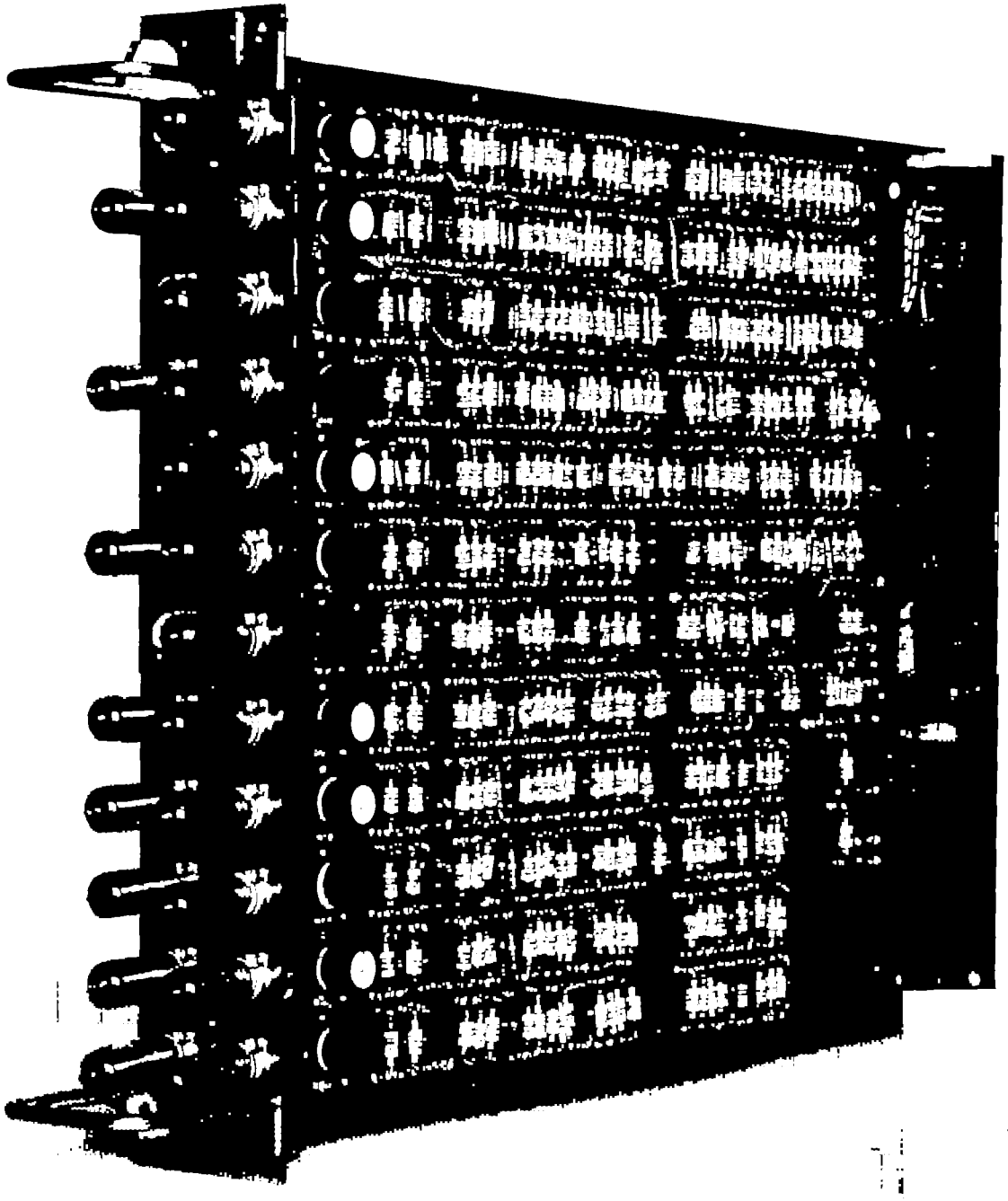


A.S.



A.S.

REF ID:A71743



A.S.